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# **Linear IFMIF Prototype Accelerator (LIPAc) Control System: Design and Development**

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# **Linear IFMIF Prototype Accelerator (LIPAc) Control System Contribution: Design and Implementation**

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*A mis padres. Por vuestros aciertos y vuestros errores, gracias.*

*A ti Sara, que estás aquí a mi lado, a tu luz.*



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# Abstract

Distributed real time control systems in scientific instruments, such as particle accelerators or telescopes, have emerged as a solution to control multiple interconnected devices, which required constant attention and observation, along with a complete integration of each of its parts. This enhancement is provided by the intense technological development that control devices have suffered in recent years. With respect to the control software, libraries and applications have also emerged in recent times. These sets of tools have been developed collaboratively in various laboratories and research centers worldwide. Experimental Physics and Industrial Control System (EPICS), a set of open source tools capable of controlling most of the devices necessary to operate a particle accelerator, can be pointed as a prime example of this progress.

This thesis presents the design and development of the EPICS based control system for Linear IFMIF<sup>1</sup> Prototype Accelerator (LIPAc), which construction involves several countries and it is currently being carried out in Rokkasho, Japan. LIPAc comprises a succession of devices and systems that focus and accelerate deuteron beam to an energy of 9 MeV with a current of 125mA, developing a previously unobtainable power of 1.125MW for that given energy. Therefore, due to the spatial charge issues associated with those beam properties, the operational requirements of such magnitudes make a complex control system but fundamental to proper operation of the prototype accelerator. LIPAc should serve as a key to demonstrate the feasibility in the construction of the IFMIF, an indispensable tool on the way to the conquest of nuclear fusion as an alternative energy source, capable of evaluating possible materials that can be used in the first nuclear fusion reactor, to be erected in the near future.

The paradigm of distributed control systems has been established within the engineering community control as a set of software and hardware technologies that provide the necessary elements for seamless integration of system components, in our case, a particle accelerator. This work presents the development of a distributed control system based on EPICS, using architectures, tools and applications that present the operation of the device as a robust set of data and variables, both accessible and understandable by engineers and operators.

The first part of this document is dedicated to review the need for nuclear fusion, framing the work presented as one of the previous steps to achieve this complex milestone. Next, a review in control systems architectures for particle accelerators is exposed. Then, it is provided an overview of current control systems with special emphasis on installations whose control is based on EPICS. Due to the large extension of the existing works, this section is not intended to be a comprehensive review, but rather a framework for establishing the context of this work and a way to highlight the most outstanding ones.

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<sup>1</sup>The International Fusion Materials Irradiation Facility, IFMIF, is an accelerator-based neutron source that will use Deuterium-Lithium stripping reactions to simulate 14 MeV neutrons from Deuterium-Tritium fusion reactions

The second part provides a description of the proposal made, which involves the design and development of a distributed control system based on EPICS. Among all kinds of control architectures, the distributed multilayer has been chosen, wherein the control system is presented as a set of hierarchical layers ranging from the resource layer, closest to the devices, until the presentation layer, closest to the operator, through the application layer. The main contribution of this proposal is the use of technology-based distributed control system over an EPICS framework, giving specific solutions to each part of the accelerator but maintaining the multi-tiered architecture. Specifically, it proposes several solutions based on the same technology software for different local control systems with the advantage of achieving a complete integration of the system and a complete understanding between all components, highlighting the development of the low level radiofrequency control system, one of the most delicate and important parts of the accelerator.

Some elements of the developed system have been tested experimentally, first instance at Ciemat facilities, using the necessary devices to simulate input data. On the other hand, the radio frequency system and its control have been tested also at high energy.

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# Resumen

Los sistemas de control distribuidos en tiempo real para grandes instrumentos científicos, tales como aceleradores de partículas o telescopios, han surgido como solución al problema de control de múltiples dispositivos interconectados que requerían una atención y observación constante, además de una integración absoluta de cada una de sus partes. Esta mejora viene proporcionada por el intenso desarrollo tecnológico que han sufrido en los últimos años los dispositivos destinados al control de sistemas. Con respecto al software de control, han aparecido en los últimos tiempos conjuntos de herramientas, librerías y aplicaciones, desarrolladas de manera colaborativa en diversos laboratorios y centros de investigación de todo el mundo. Como máximo exponente de este progreso está EPICS, un conjunto de herramientas Open Source, capaz de controlar la mayoría de los dispositivos necesarios para hacer funcionar un acelerador de partículas.

En esta tesis se presenta el diseño y desarrollo del sistema de control, basado en EPICS, del acelerador lineal prototipo IFMIF, LIPAc en inglés, en cuya construcción participan varios países, llevándose a cabo en Rokkasho, Japón. LIPAc está compuesto por una sucesión de sistemas y dispositivos que focalizan y aceleran un haz de deuterones hasta una energía de 9 MeV con una corriente de 125mA, desarrollando una potencia nunca antes conseguida, con dicha energía, de 1.125MW. Por tanto, los requisitos operacionales derivados de tales magnitudes y de la carga espacial asociada, hacen del sistema de control un elemento complejo pero fundamental para el correcto funcionamiento del acelerador prototipo. LIPAc debe servir como elemento clave para demostrar la viabilidad de la construcción de IFMIF, una herramienta indispensable en el camino hacia la conquista de la fusión nuclear como fuente alternativa de energía, capaz de evaluar posibles materiales que puedan ser utilizados dentro del primer reactor nuclear de fusión, que se erigirá en un futuro próximo.

El paradigma de los sistemas de control distribuidos se ha establecido dentro de la comunidad de la ingeniería de control, como el conjunto de tecnologías tanto software como hardware que pretenden proporcionar los elementos necesarios para conseguir una total integración de los sistemas que componen en este, nuestro caso, un acelerador de partículas. En el presente trabajo se propone el desarrollo de un sistema de control distribuido basado en EPICS que utilice arquitecturas, herramientas y aplicaciones que muestren el funcionamiento del artefacto como un conjunto robusto de datos y variables, accesibles y entendibles tanto por los ingenieros como por los operadores.

La primera parte del documento se dedica a revisar, en primer lugar, la necesidad de la energía nuclear de fusión, enmarcando el trabajo presentado como una de los pasos previos para conseguir este complejo hito. Seguidamente, se ofrece una visión general de arquitecturas de sistemas de control actuales en aceleradores de partículas, haciendo especial hincapié en aquellas instalaciones cuyo control está basado en EPICS. Debido a la gran extensión de los trabajos existentes, esta sección no pretende ser una revisión exhaustiva, sino un marco para establecer el contexto de esta tesis y una forma de resaltar los trabajos más destacados.

La segunda parte proporciona una descripción de la propuesta realizada, que consiste en el diseño y desarrollo de un sistema de control basado en EPICS. Entre todos los tipos de arquitecturas de control se ha optado por seguir el modelo distribuido multicapa, en el cual el sistema de control se presenta como un conjunto de estratos jerarquizados que van desde la capa de recursos, la más cercana a los dispositivos, hasta la capa de presentación, la más cercana al operador, pasando por la de aplicación. La principal aportación de la propuesta es el uso de la tecnología de sistemas de control distribuidos basados en EPICS que da solución específica a cada parte o subsistema del acelerador, manteniendo siempre la arquitectura multicapa. En concreto se proponen diversas soluciones basadas en la misma tecnología software para los diferentes sistemas de control locales del acelerador, con la ventaja de conseguir una integración absoluta del sistema y un entendimiento completo entre todas las partes que lo componen; destacando en esta segunda parte, el desarrollo del control del sistema de radiofrecuencia a bajo nivel, una de las partes más delicadas e importantes del acelerador.

El sistema desarrollado se ha probado en primera instancia de forma experimental en los bancos de pruebas de las instalaciones del Ciemat, utilizando los dispositivos necesarios para simular datos de entrada. Por otro lado, el sistema de radiofrecuencia y su control han sido además evaluados en tests a altas energías.

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# 1

## Introduction

*Observar y razonar son dos constantes en mi vida que no puedo dejar, querido Watson.*  
Sherlock Holmes.

In this first chapter, context of the problem and its motivation are presented in section 1.1. Next, in section 1.2, a general approach is shown. Problem formalization is presented in section 1.3. Finally, in section 1.4, the structure of the document is described.

### 1.1 Context of the problem and motivation

Without control systems there could be no manufacturing, no vehicles, no computers, no regulated environment, in short, no technology. Control systems are what make machines, in the broadest sense of the term, to work as intended. Control systems are most often based on the principle of feedback, whereby the signal to be controlled is compared to a desired reference signal and the discrepancy used to compute corrective control action [15] [16] [17].

The first control systems were developed during the industrial revolution at the end of the 19th century. The control function was implemented by using ingenious mechanical devices automating some of the most repetitive and critical tasks on the assembly lines. These devices had to be individually adapted to each task and due to their mechanical nature they also suffered from a short life-time.

In the 1920s, mechanical control devices were replaced by electrical relays and connectors. Relay logic made it possible to develop larger and much more sophisticated control functions. Since then, electrical relays have been used in a large number of control systems around the world. Relays have proven to be a very cost-effective alternative, especially for automating small machines with a limited number of transducers and actuators.

In today's industry, relay logic is rarely chosen for new control systems but a large number of older systems are still in use. The silicon-based integrated circuit (IC), paved the way for a new generation of control systems in the 1970s. Compared with relays, ICs based on transistor-transistor logic (TTL) or complementary metal-oxide-semiconductor (CMOS) integrated circuits are much smaller, faster and also have a longer lifetime. In most control systems based on relays and ICs, the control algorithm is permanently defined by the electrical

wiring. Systems with wired logic are easy to implement but unfortunately it is difficult and time-consuming to change their behavior.

In the early 1970s, the first commercial computers debuted as controllers in large control systems. Since computers can be programmed they offer a great advantage compared with the wired logic function in systems based on relays or ICs.

A linear accelerator is an electric device that greatly increases the velocity of subatomic particles or ions along a linear beamline [18] [19]. In order to control and operate these kind of machines, distributed control systems, see section 3.2.3, have proven particularly useful, because they provide the possibility of comprising tens or even hundreds of computers, networked together to allow communication between them and to provide control and feedback of the various parts of the device from a central control room, or even remotely over the internet. In a distributed control system, controllers are provided locally to systems or groups of devices, but networked to one or more operator stations in a central location through a digital communication circuit.

On the way to nuclear fusion there are several milestones, the IFMIF project, a linear accelerator-based neutron source, is a crucial one, see section 2.3. The objective of IFMIF is to gain the knowledge in radiation effects materials for the design of a demonstration fusion power plant. For the validation of the IFMIF accelerator facility, LIPAc (Linear IFMIF Prototype Accelerator) is being carried out. LIPAc is capable of generating, accelerating and transporting an intense deuteron beam in continuous wave mode and it corresponds to the IFMIF low-energy accelerator.

Fig. 1.1 (top) shows the generalized Perveance  $K$ , relevant for judging space-charge forces as a function of beam energy for the most powerful accelerators, while Fig. 1.1 (bottom) gives for the same accelerators the beam power. For a given energy, IFMIF and accordingly LIPAc, have the highest beam power and the highest space charge regime. The beam power becomes critical from the point of view of losses, that means when the beam power becomes so high, it must be precisely controlled, even tiny losses as low as  $10^{-6}$  of the beam must be avoided to allow hands-on maintenance. This fact requires developing a coherent strategy when designing and optimizing the accelerator control system, where several innovative procedures must be developed. A global strategy for the LIPAc control system development is thus necessary, making it the main issue to be addressed in the presented work.

As a result, LIPAc control system is designed to convey all monitor, control, model-based, and computed data from all accelerator, facility, experimental, safety, and operations subsystems to accomplish supervisory control, automation, and operational analysis. The scope of the control system extends from the interface of the equipment being controlled through, to the designers and operators of the accelerator facility, as well as accelerator beamline experimenters and staff. LIPAc control system includes all hardware and software for global systems such as timing, deterministic data communication, network communication, control room operations, automation and optimization. Being EPICS, see section 4.2, the primary tool used for the design and development of control system.

Hence, the main motivation and contribution of this work is the design and development of some parts of the LIPAc control system.

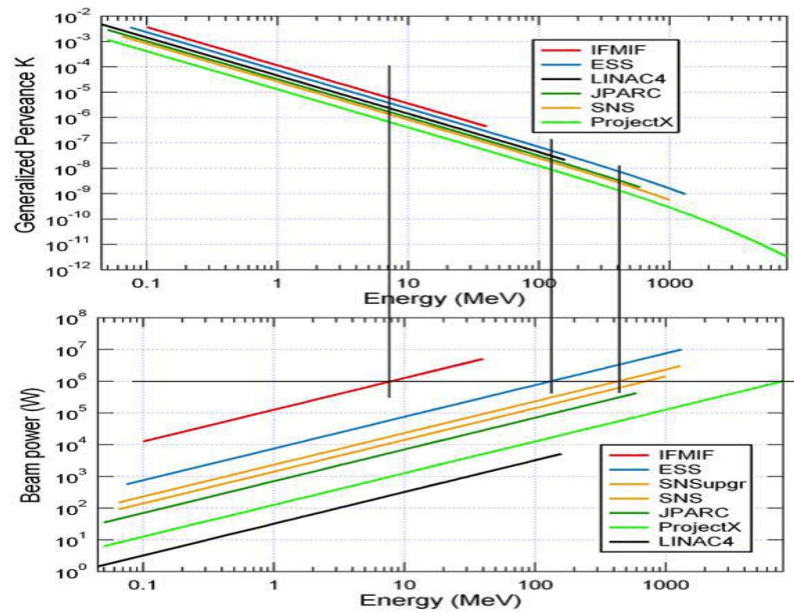


Figure 1.1: Linear accelerators energy comparison

## 1.2 General approach and objectives

Some instruments can be characterized as having essentially a monitoring function. Thermometers, barometers and anemometers are used for this purpose, they simply indicate the condition of the environment, and their readings cannot be used as a control function in the ordinary sense. Therefore, the monitoring process would not define a control system.

The external input of a system is called the reference. When one or more output variables of a system need to follow a certain reference over time, a controller manipulates the inputs to a system to obtain the desired effect on the output of the system. According to this, a control system of a complex process must ensure the following requirements:

**Reliability:** It is one of the main features of any control system. Be reliable involves all phases and components thereof, from direct measurement of the process by sensors, to actuators, passing through all the equipment comprising that system.

Reliability depends on many factors, most of which can be controlled, but not others related to natural disasters or intentional accidents. A more reliable system can be done, instead of placing a single controller, two controllers, in this case, if one fails, the other takes over.

**Security:** A control system must be safe, the safety concept applied to a control system is linked to all that encompasses, from the protection of the elements that compose it, to the protection of human life. A control system must be designed to protect the environment as well.

**Versatility:** Although a control system is designed based on initial features and specifications, it must have the ability to adapt to changes and modifications. For example, if it is decided to enlarge the capacity of a plant, the system should allow to enter new control

variables without affecting the overall performance of the entire operation. The system must also have the ability to integrate to its control, equipment and instruments of different brands and manufacturers, consisting of electronic and various operating systems.

**Performance:** When a system meets the aforementioned properties, it is then possible to start thinking about their performance. Performance in control systems for accelerators mostly refer to processing speed and management of large amounts of data. A control system must take full advantage of the available resources in order to minimize expenses. The current economic situation and the high cost of large scientific projects currently require that accelerator control systems are able to reuse and share resources across the entire line.

**Speed:** This feature allows the system to act more quickly in situations that require it, such as risk ones for the machine itself or staff. The speed is closely related to communication speed transmission and reception of data between the different subsystems that make up the system

**Manageable:** control systems like any other technology, are designed to facilitate the task of the human being, improving productivity and replacing him at risk. For this reason should be designed to be operated with ease, with man-machine interfaces that simplify operation and allow the understanding of the process through visualization.

In order to develop a control system that meets the requirements outlined above and to demonstrate its validity on a linear particle accelerator, following [15], it is proposed:

- Study the system to be controlled and decide what types of sensors and actuators will be used and where they will be placed.
- Model the resulting system to be controlled.
- Decide on performance specifications.
- Decide on the type of controller to be used.
- Design a controller to meet the specs, if possible; if not, modify the specs or generalize the type of controller sought.
- Simulate the resulting controlled system, either on a computer or in a pilot plant.
- Choose hardware and software and implement the controller.
- Tune the controller if necessary.

The components of a particle accelerator can be divided up into a number of different subsystems, depending on the functional use of them. Some of these subsystem classifications are very easy to work with and have a large theory base for analysis, [20] [21]. LIPAc accelerator system classification has been established following the structure defined in other similar accelerators, [21] and [22], it is as follows:

- Injector
- Radio Frequency Quadrupole (RFQ)

- Medium Energy Beam Transport (MEBT)
- Superconducting Radio Frequency (SRF) Linac
- High Energy Beam Transport (HEBT) & Beam Dump (BD)
- Beam Instrumentation (BI)
- Radio Frequency (RF) power system
- Control system

Each of these items, except control system, is considered a subsystem within the accelerator system and each one has a Local Control System (LCS) associated. Control system and LCSs are in charge of the whole accelerator control, playing different roles and functions that will be detailed later. Taking into account this design, the operation requirements outlined above and the inherent characteristics to a control system of a large facility such as a particle accelerator, the main objectives of the work presented in this thesis are:

- To carry out the design and development of the local control system associated to the next subsystems: MEBT, SRF Linac, HEBT & BD, RF system and BI.
- To achieve the design and development of the Low Level Radio Frequency (LLRF) control system to be implemented in the RF LCS.
- To contribute to the design on the Machine Protection System (MPS), Personal Protection System (MPS) and the Central Control System (CCS), as elements of the control system, in the aspect related to the previously mentioned subsystems.

Another requirements to be fulfilled by the work developed in this thesis are:

- The developed control system must be able to operate in a harsh environment without losing efficiency and processing speed, any fault in any part of the accelerator must be recorded and identified unequivocally instantaneously.
- Control information must be available for all subsystems.
- Each local control system has to deal with the entire subsystem to which it belongs and has to have knowledge of the operation of all devices in this subsystem.

## 1.3 Problem formalization

A synthesis problem is a theoretical problem, precise and unequivocal. Its objective is mainly pedagogical: It gives something clear to focus on for the purpose of study. The hope is that the principles learned from studying a formal synthesis control problem will be useful when it comes to designing a real control system [23].

Following [24], the objective in a control system is to make some output, say  $y$ , behave in a desired way by manipulating some input, say  $u$ . The simplest objective might be to

keep  $y$  small (or close to some equilibrium point), a *regulator problem*, or to keep  $(y - r)$  small, for  $r$ , a reference or command signal, a *servomechanism or servo problem*. In order to know what is small for a signal, it is fundamental to introduce criterion for signals; then  $y$  *small* means  $|y|$  *small*. Which criterion is appropriate depends on the particular application. In summary, performance objectives of a control system guide to the introduction of norms; then, specifications are given as norm bounds on certain key signals of interest.

As exposed in [15], the most general block diagram of a control system is shown in Fig. 1.2. The generalized plant consists of everything that is fixed at the beginning of the design: actuators, sensors measuring certain signals, analog-to-digital and digital-to-analog converters, and so on. The controller consists of the configurable part: it may be an electrical board, a programmable logic controller, an embedded PC, a general-purpose computer, or some other modifiable device.

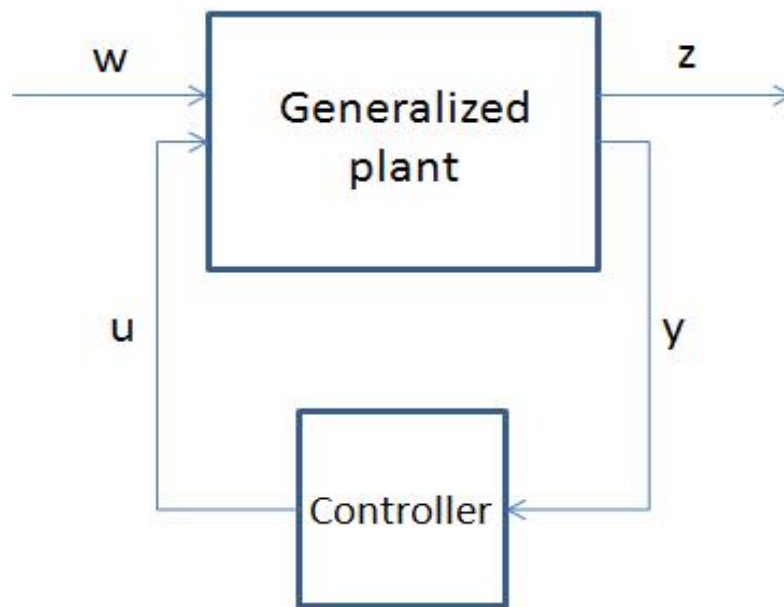


Figure 1.2: Most general control system

The signals  $w$ ,  $z$ ,  $y$ , and  $u$  are vector-valued functions of time. The components of  $w$  are all the external inputs: references, disturbances, sensor noises, and so on. The components of  $z$  are the signals we would like to control: tracking errors between reference signals and plant outputs, actuator signals whose values must be kept between certain limits, etc. The vector  $y$  contains the outputs of all sensors. Finally,  $u$  contains all controlled inputs to the generalized plant.

Not very often is the external input  $w$  a fixed, known signal. Usually,  $w$  is not fixed but belongs to a set that can be characterized in some way:

- In a temperature regulator, the reference signal is always constant: at certain times during the day the thermostat is set to a new value. The temperature of the outside air is not constant but varies slowly within limits.

- In a vehicle such as an airplane or ship the pilot's commands on the steering wheel, throttle, pedals, and so on come from a predictable set, and wave motions have amplitudes and frequencies that can be defined with some degree of reliance.

In particle accelerators control systems, external inputs and experiences from the past must be considered. The ultimate target for any control system is to seek the right properties and desired values for  $z$ . For this, it is necessary to act in coordination between the systems and subsystems, in order to make  $z$  more uniform and accordingly, to improve the final challenge of the entire facility [15].

## 1.4 Document structure

This document is divided into two main parts. First one consists on a description of the current state in nuclear fusion and control systems in particle accelerators. Specifically, chapter 2 gives a description of the international nuclear fusion framework and the IFMIF facility, explaining its context in this work in section 2.3. A characterization of control systems architectures and its role in some large relevant processes is offered in chapter 3. Chapter 4 ends the background part with a depiction of EPICS based control systems, showing some pertinent examples of facilities using EPICS, section 4.3.

The second part of the document consists of the contributions made and the solutions that have been applied to perform the LIPAc control system. Chapter 5 gives a deep explanation of each part of the accelerator and how the control system has been designed to achieve the operating requirements of LIPAc. One of most important portion of LIPAc is the LLRF system, thus, the solution developed to its control system is explained in chapter 6. chapter 7 shows the tests that have been conducted both in the LLRF system test bench and in the RF prototype chain with the LLRF system installed on it.

Finally, a summary of the main thesis contributions together the most relevant conclusions is presented. References are shown at the end of the document.







---

**Background**



---

# 2

## The need of nuclear fusion

*Es estúpido pedir a los dioses las cosas que uno no es capaz de procurarse a si mismo.*  
*Sentencias Vaticanas, Epicuro.*

### 2.1 Introduction

Following C.L Smith [1], the International Energy Agency (IEA) predicts that energy use will increment 60% by 2030 and double around 2045. 80% of the consumed energy is derived from fossil fuels. This is instigating a potentially climate change and generating pollution. Therefore, it is urgent to find alternatives, besides the fact that fossil fuels will eventually run out.

Since the industrial revolution, the atmosphere is being threatened by the increase of  $CO_2$ , Fig. 2.1. The result appears to be an increase in the average global temperature, Fig. 2.2.

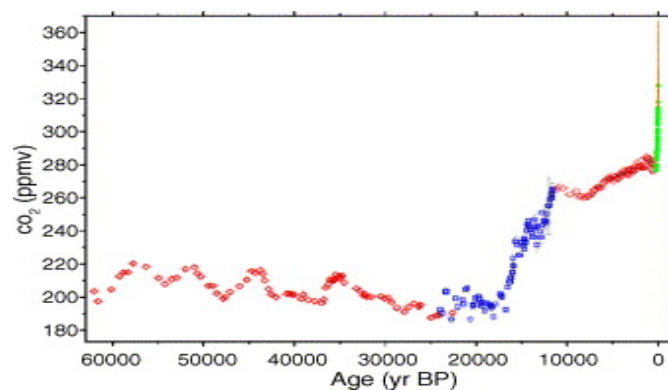


Figure 2.1: Atmospheric concentration of  $CO_2$  (in parts per million by volume) over the last 60,000 years [1]

The pretentious target of limiting atmospheric  $CO_2$  to 500 ppm by 2050 is commonly cited, this fact would improve the situation but it would not remove all obstacles. The US Department of Energy estimates that in order to meet this goal, 20 TW, of the predicted total world power consumption of 30 TW, would have to be produced without  $CO_2$ . This

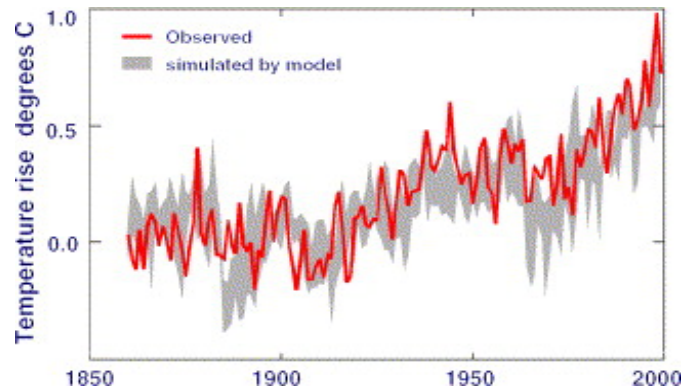


Figure 2.2: Observed average global temperature over the last 150 years compared to model simulations [1]

20 TW is almost 50% more than today's total power market (of 14 TW). To quote the US Department of Energy *the technology to generate this amount of emission-free power does not exist* [1].

At current rates of consumption, it is assumed that there is enough coal for several hundred years and enough gas for about 150 years. There are also huge amounts of *unconventional* oil (shale and tar sands), which however would be very expensive to convert to usable forms, both in terms of the cost and in terms of  $\text{CO}_2$  production and energy.

After stating the current energy problem, the rest of the chapter tries to frame the presented work in the context of nuclear energy, emphasizing the nuclear fusion as possible alternative to fossil fuels in section 2.2. In addition, it is considered desirable to provide an explanation about the international current situation regarding to fusion energy, section 2.2.1 and section 2.2.2. Besides, throughout this chapter, one of the most important challenges involved in the current scenario of nuclear fusion energy, IFMIF, is introduced in section 2.3. The chapter ends with a brief summary, section 2.4.

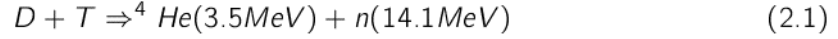
## 2.2 Nuclear fusion

Nuclear Fusion is the energy-producing process which takes place continuously in the Sun and stars. In the core of the Sun at temperatures of 10-15 million  $^{\circ}\text{C}$ , hydrogen is converted to helium providing enough energy to sustain life on Earth. For energy production on earth different fusion reactions can be used. The most suitable reaction occurs between the nuclei of the two heavy forms (isotopes) of hydrogen - deuterium (D) and tritium (T); eventually reactions involving just deuterium or deuterium and helium ( $3\text{He}$ ) may be used.

At the temperatures required for the D-T fusion reaction - over 100 Million  $^{\circ}\text{C}$  - the fuel has changed its state from gas to plasma. In a plasma, the electrons have been separated from the atomic nuclei (usually called the *ions*). Plasmas are now used widely in industry, especially for semi-conductor manufacture.

A mix of deuterium (D) and tritium (T) at a temperature of two hundred million degrees centigrade will produce fusion reactions to generate 10 to 50 times more energy the power

needed to maintain the reaction. An equation of such a fusion reaction is showed here:



In view of the fact that tritium is not available in nature in sufficient quantities, it must be regenerated inside the thermonuclear reactor. This is achieved by letting neutrons, originating from fusion reactions, collide with lithium (Li) nuclei, thus inducing the following nuclear reactions:



Nuclear fusion offers a vast, new source of energy with plentiful fuels. It is inherently safe since any malfunction results in a rapid shutdown. There is no atmospheric pollution leading to acid rain or *greenhouse* effect. Radioactivity of the reactor structure, caused by the neutrons, decays rapidly and can be minimized by careful selection of low-activation materials. Provision for geological time-span disposal is not needed. Deuterium fuel is abundant as it can be extracted from all forms of water. If all the world's electricity were to be provided by fusion power stations, deuterium supplies would last for millions of years. Tritium does not occur naturally and will be manufactured from Lithium [25] [26] within the machine. Lithium, the lightest metal, is plentiful in the Earth's crust. If all the world's electricity were to be provided by fusion, known reserves would last for at least 1000 years. The by-product, helium, has no role in nuclear weapons production.

### 2.2.1 Nuclear fusion and the European Fusion Programme

Progress towards the achievement of fusion as an inexhaustible energy source that is respectful with the environment has received a strong impulse with the agreement between Europe, USA, Japan, Russia, China, South Korea and India, on the construction of the experimental device [27] [28] ITER, meaning The Way in Latin, at the french site of Cadarache.

These governments, representing more than half of the world population, will contribute a total of 15.000M€ over a period of 20 years to the construction and exploitation of ITER, whose main goal is to demonstrate that controlled fusion can be achieved scientifically. ITER is a device of the tokamak type, in which intense magnetic fields confine a toroidally shaped plasma.

ITER will demonstrate the scientific viability of controlled fusion, but the commercial generation of electricity based on thermonuclear fusion will require the prior solution of a number of technological problems. One of the main remaining issues are related to materials, which must be capable of withstanding radiation and large thermal loads, remotely controlled maintenance systems needed to guarantee the availability of the plant, and tritium regeneration systems to guarantee self-sufficiency. The solution of these critical issues is required to demonstrate the technological viability of fusion.

Some of these issues require implementing large-scale projects. The most important of these are:

1. IFMIF (International Fusion Materials Irradiation Facility), see section 2.3, an installation for testing materials that will be used in a fusion reactor.
2. JT60-SA [29], a superconducting tokamak that will allow experimenting with alternative concepts for the operation of ITER.

If all these projects, namely ITER, IFMIF and JT-60, materialize over the next 10 years, a prototype fusion reactor will be built, called DEMO (DEMONstration Fusion Power Reactor) [30] [31] [32].

The above indicates that the coming decades will experience large advances in thermonuclear fusion research and associated technologies, while shifting the main focus from basic research in plasma physics to the technological development of all the constituent systems of a fusion reactor, which will require planning and implementing large multinational projects.

### 2.2.2 The long-term european fusion programme

The long-term european programme includes activities that are not directly related to ITER yet considered indispensable for the development of the future fusion reactors. In order to define the scope of these activities, an evaluation was made of the specifications of the future fusion reactor. This study, known as the *European Power Plant Conceptual Study* (PPCS) [33] [34], described four different types of fusion reactors with varying degrees of technological complexity and efficiency. The long-term european programme was defined on the basis of the research and development needs identified in that work. Its main points are, first, the development and characterization of functional and structural materials required for the various fusion reactor concepts, and their validation at the IFMIF high intensity neutron source, having a spectrum similar to that expected in a fusion reactor. Second, the validation of the fuel cycle, with special emphasis on tritium control, and finally, the development and validation of remote handling components, indispensable for any future fusion power plant [35].

### 2.2.3 Fusion materials

In the long-term european programme, materials activities [36] are mainly concentrated on the study and characterization of EUROFER [37], ferritic-martensitic [38] low-activation steel that will constitute the main structural material of DEMO. It is important to emphasize that the exposure to radiation inside fission reactors only provides qualitative information on radiation damage, as the radiation in a fusion reactor will generate Hydrogen (H) and Helium (He) inside the material, so that the damage needs to be verified using a neutron source with a spectrum similar to the spectrum corresponding to the future reactors.

Other interesting materials consist of tungsten (W) and its alloys [39]. Recently, these materials have received more attention due to their possible application in high-temperature

He cooled divertors. In such divertors, a heat flux of the order of  $10\text{MW}/\text{m}^2$  must be extracted, requiring highly pressurized He at a high temperature. The only material able to withstand such conditions is tungsten, in spite of its low ductility, its high ductile-fragile transition temperature and the complications it presents for mechanization purposes.

Another activity that has gained prominence in the materials area of the long-term european programme is the first-principles based modeling of irradiation effects [40]. Over the last 15 years, the availability of increasing computing power in supercomputer centers, and the development of new algorithms, has given rise to a new branch of science that studies the behaviour of materials on the basis of the simultaneous simulation of millions of particles. The simulating radiation effects in Fe and, more recently, in Fe and Cr. It is to be expected that the scope of these studies will be broadened to include the various components of the EUROFER steel and other materials, such as Oxide-Dispersion-Strengthened (ODS) and  $\text{SiC}_f/\text{SiC}$ , in the near future. It should be emphasized that this activity is essential for the interpretation and the comparison of the results that are currently being obtained from radiation exposure experiments in fission reactors, and the future results that will be obtained at IFMIF.

## 2.3 International Fusion Materials Irradiation Facility (IFMIF)

As mentioned above, the main motivation of this work arises from the design and development of LIPAc control system, being LIPAc the prototype particle accelerator of IFMIF. Therefore, it is considered appropriated to give an overview of this future installation, IFMIF, its main objectives, history and the IFMIF-EVEDA phase, where LIPAc is settled.

### 2.3.1 Introduction

Irradiation environment in the future fusion power plants (and obviously also in DEMO independently of its specific design) is characterized by the presence of 14 MeV neutrons in the first wall area. Understanding the degradation of the materials and components properties throughout the reactor operational life is a key issue to allow the design and subsequent facility licensing by the corresponding safety authorities.

The presence of radiation-induced defects, He or, to a lower extent, H in the reactor, can significantly affect its material properties and it is also well known, from a qualitative point of view, that there are very significant synergetic effects. Unfortunately, the detailed information of these effects, needed for the engineering design of DEMO as well as a fusion reactor, is missing, especially for structural materials [41], mainly due to the lack of enough experimental data that should be produced through testing in as close as possible conditions [42], [43] to fusion environment.

These experimental data can only be produced using some kind of irradiation source, and there is general consensus that the available (fission, spallation and ion beam) irradiation sources do not have the proper characteristics to fulfill the observed needs. Intense neutron sources, like fission reactors or spallation sources are not fully fitting to fulfill the characteristics of a fusion neutron source due to the very different He and H to dpa rate (very low

He/dpa and H/dpa in the case of the fission reactors and very high He/dpa and H/dpa in the case of spallation sources).

The main requirement for the desired neutron source is to produce fusion characteristic neutron spectrum [44] with enough intensity to allow accelerated testing, up to a level above the expected operational lifetime, with an irradiation volume large enough to permit the characterization of the macroscopic properties of the materials of interest required for the engineering design of DEMO [30].

### 2.3.2 The IFMIF History

The need of a fusion relevant neutron source was clear from the start of the nuclear fusion developments. Intense discussions over the years concluded in the consensus driven by the material scientist community that an accelerator-based source utilizing deuterium-lithium nuclear reaction with a broad energy spectrum peaked at around 14 MeV would be the best choice for a materials irradiation facility [45].

A high neutron flux, being correlated with the deuteron current, demands high availability [46] [47] [48] of the facility to produce the fusion materials database on a time scale consistent with anticipated DEMO construction. This source was called IFMIF. It will achieve this targets using two 40 MeV deuteron linear accelerators [49], each delivering a 125 mA beam current with 100% duty cycle. Both beams strike a flowing lithium target, hence providing an intense neutron flux density of about  $10^{18} n/m^2s$  with a broad energy peak near 14 MeV, Fig. 2.3.

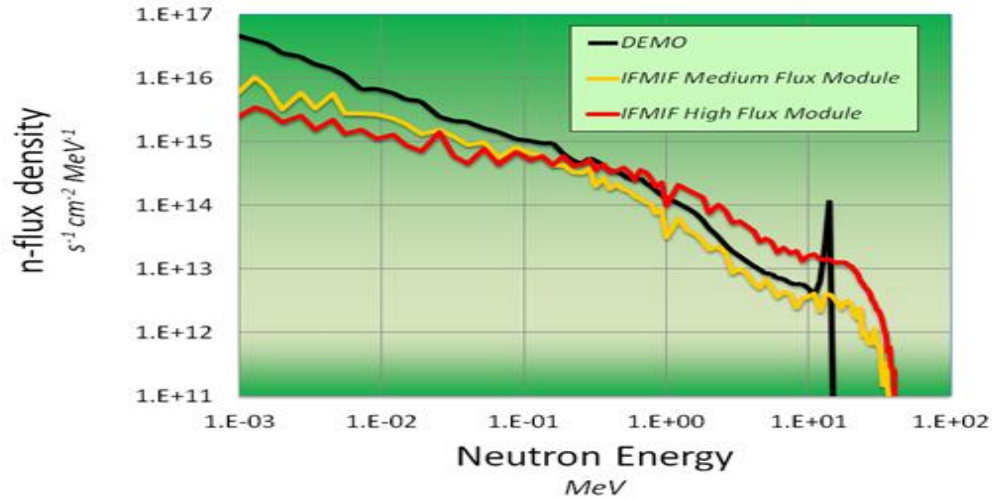


Figure 2.3: DEMO VS IFMIF flux density

In the period from 1990 to 2006, IFMIF was a joint effort of the European Union (EU), Japan, the Russian Federation (RF), and the United States of America (USA) within the framework of the Fusion Materials Implementing Agreement of the IEA.



A reference conceptual design [50] and a cost estimate [51] for IFMIF were developed during the *Conceptual Design Activity* (CDA) phase (1995-96). That design was the basis for the *Conceptual Design Evaluation* (CDE) phase (1997-98) [52]. In 1999, the IEA Fusion Power Coordinating Committee (FPCC) requested a review of the IFMIF design, and directed that it had to be focus on cost reduction [53] [54] without changing the original mission. In addition, the concept of staged deployment of the facility was also suggested to reduce the initial investment and to lower the annual expenditures during construction.

The *Key Element Technology Phase* (KEP), during 2000-2002, was carried out with the objectives of reducing some of the key technology risk factors on the path to achieve a continuous deuteron beam with the desired current in the accelerators, to verify relevant component designs on a laboratory scale (both in the lithium target system and test facilities), and to validate design codes. The EU, Japan, RF and USA contributed to perform different KEP tasks.

Finally a Comprehensive Conceptual Design Report (CDR) [55] was produced in 2004 summarizing the technology level and the estimated costs of the major systems at that time, based on the results of the CDA, CDE and KEP phase and proposing an R&D program for the next step of the project: the Engineering Validation and Engineering Design Activity (EVEDA) [2].

### 2.3.3 IFMIF Requirements

The mission of IFMIF is thus to provide a neutron source producing high energy neutrons at sufficient intensity and irradiation volume to:

- Generate materials irradiation test data for design, licensing, construction and safe operation of fusion demonstration reactor, DEMO, under simulated fusion environment up to about full lifetime of anticipated service in DEMO.
- Serve as a source of material and sub-component irradiation test data characteristic to fusion power plants.
- Generate a database for benchmarking of radiation responses of materials hand in hand with computational material science.

This mission imposes a set of requirements on the design of the source, which can be summarized as follows:

1. The neutron spectrum must be similar to that of a fusion reactor, as the effect of neutron radiation on materials depends critically on the neutron energy. More specifically, the parameter commonly used to express radiation effects is the ratio between the number of He atoms generated via nuclear reactions and the number of ions displaced from their position in the matrix (know as dpa).
2. The nature of the interaction with the material ions is of fundamental importance. Due to their interaction with the incident particles, the materials ions receive an amount

of energy that displaces them from their initial position (recoil atoms). The energy spectrum of such recoil atoms determines the type of defects that are produced in the material.

3. The radiation source must be continuous, since it is not evident that a pulsed radiation source produce equivalent effects.
4. The source must be capable of generating a dose equivalent to 150 dpa in a significant irradiation volume over a few years. This means that high neutron fluxes are required (of the order of  $5 \times 10^{17} \text{ n/m}^2\text{s}$ ) and that the device must operate with a high degree of availability (of the order of 70%). In addition, it must allow access to the irradiation zone, as it may be necessary to control the temperature and the atmosphere, or to perform *in-situ* experiments and measurements.

### 2.3.4 IFMIF Plant configuration

IFMIF Plant is defined to provide an accelerator-based D-Li neutron source to produce high energy neutrons at sufficient intensity and irradiation volume to simulate as closely as possible the first wall neutron spectrum of future nuclear fusion reactors.

This design incorporates two high intensity deuteron accelerators -about 125 mA each- with an energy of 40MeV, impinging on a liquid Li target. Via nuclear *stripping* reactions a neutron spectrum is obtained with parameters suitable for the majority of the cited materials studies. The IFMIF accelerators have been defined and detailed [2] and most of the involved technologies are being manufactured and tested during the EVEDA phase at LIPAc

The installation will consist of three main areas and two secondary areas. The main areas are: the set of two accelerators, the target zone, and the irradiation zone. The secondary areas are: hot cells to analyze the samples after irradiation, and conventional installations. Fig. 2.4 shows a view of the resulting design [56].

The IFMIF systems needed to fulfil a common goal have been grouped in the so-called facilities Fig. 2.5. The systems devoted to produce the high power beams are grouped in the Accelerator Facility (AF), the systems related to the lithium target management constitute the Lithium Target Facility (LF), the systems in charge of the irradiation modules handling and management compose the Test Facilities (TF), the Post Irradiation Examination Facility (PIEF) includes the systems in charge of the analysis of irradiated specimens, and finally, the Conventional Facility (CF) provides power, cooling, ventilation, rooms and services to the other facilities and itself.

#### 2.3.4.1 Accelerator Facility (AF)

The main functions of the AF are produce the D+ beams, accelerate, transport and shape the beams and direct them to the Li Target.

The AF includes two accelerators and some specific auxiliaries necessary to operate. Each IFMIF accelerator is a sequence of acceleration and beam transport stages. It must be noted that the configuration of the two accelerators is the same. Top-level performance requirements for the IFMIF accelerators can be observed in Table 2.1.

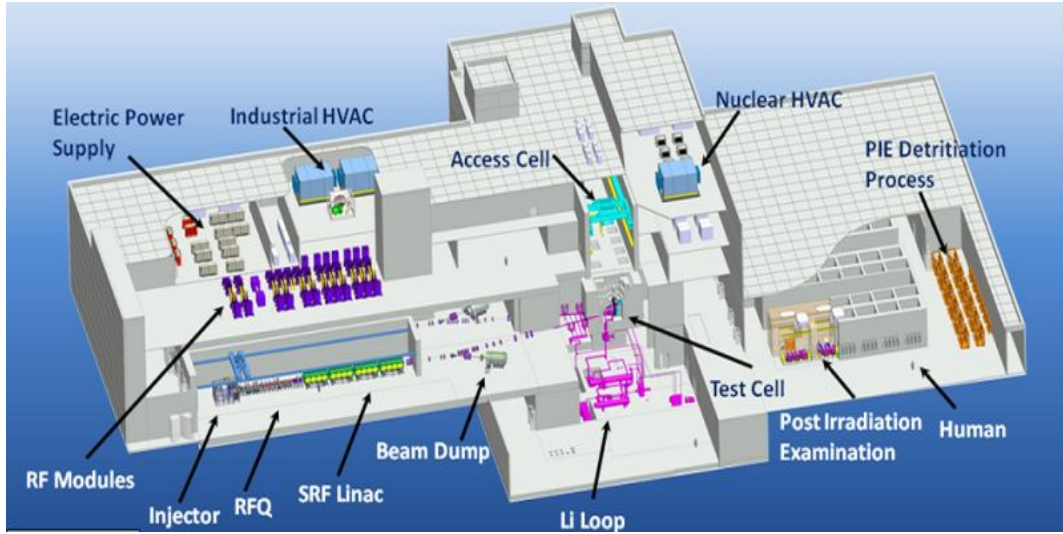


Figure 2.4: 3D view of the IFMIF facility for materials irradiation

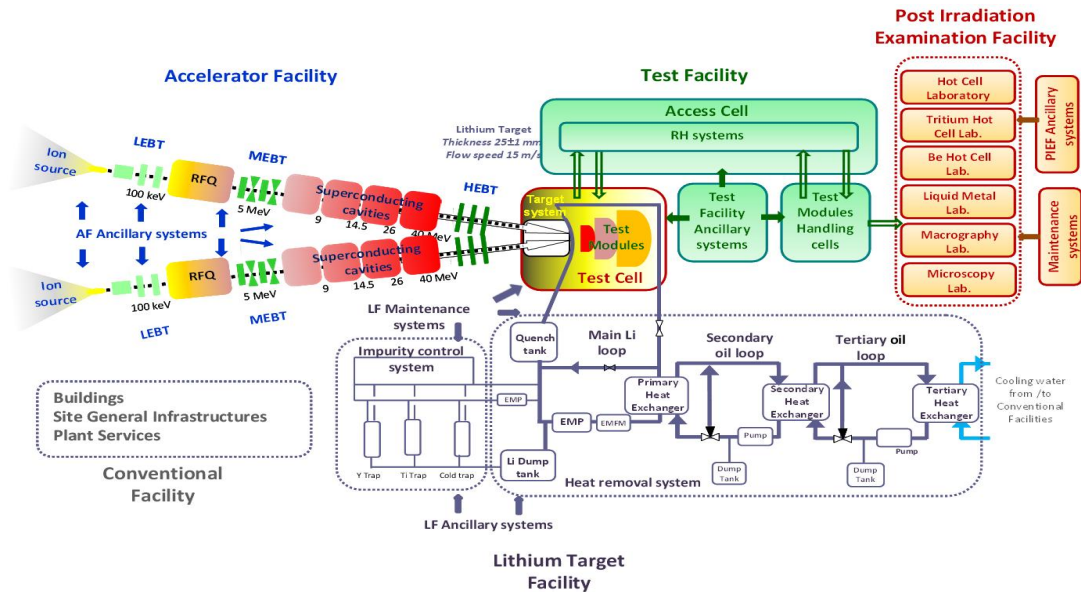


Figure 2.5: Schematic view of the different facilities [2]

First, an Electron Cyclotron Resonance (ECR) ion source creates a continuous wave 140 mA deuteron beam, which is extracted by an extraction system based on five electrodes which accelerates particles up to 100 keV. A Low Energy Beam Transport (LEBT) line guides the beam with solenoids and injects it properly into the Radio Frequency Quadrupole (RFQ). Both the ECR and the LEBT belongs to the Injector system.

The RFQ bunches and accelerates the beam from 100 keV to the energy of 5 MeV, and its output beam is injected in the following Medium Energy Beam Transport line (MEBT) line, which conditions the beam in transverse with quadrupoles and in longitudinal with buncher

Table 2.1: Top-level performance requirements for the IFMIF accelerators

Top-level performance requirements for the IFMIF accelerators		
Requirement	Specification	Detail-Comment
Particle type	$D^+$	$H_2^+$ for testing (avoids activation)
Accelerator type	rf linac	175 MHz, 5 MeV RFQ followed by 5-40 MeV, 175Mhz DTL
Number of accelerators	2	Parallel operation
Output current	250 mA	125 per accelerator (independent operation)
Beam distribution	rectangular flat top	20 cm horizontal x 5 cm vertical
Output energy	40 MeV	User requirement
Output energy dispersion	$\pm 0.5$ MeV FWHM (full width at half maximum)	Target requirement
Duty factor	CW	Pulsed tune-up and start-up
Availability	$\geq 88\%$	During scheduled operation
Maintainability	Hands-on	For accelerator components up to final bend in HEBT with local shielding as required; design not to preclude capability for remote maintenance
Design lifetime	30 years	

cavities, in order to properly inject it into the Superconducting Radio Frequency Linear Accelerator (SRF Linac).

The SRF Linac, composed of 4 cryomodules (sets of superconducting accelerating cavities and solenoid), accelerates the beam up to a final energy of 40 MeV.

Finally, the High Energy Beam Transport (HEBT) line, comprised of a series of magnetic optics elements, is required to tailor the beam to provide the flat rectangular beam profile (200 mm x 50 mm) on the flowing lithium target, Fig. 2.6, [57].

In addition, during the phases of commissioning and beam characterization or tuning at restart it is necessary to steer the beam from the main line towards a Beam Dump (BD), consisting basically of an actively cooled cartridge which stops the beam, and a local shielding to attenuate the resulting radiation. Each accelerator will have its own dedicated Beam Dump installed in an adjacent line of the HEBT.

The RFQ and SRF Linac accelerating structures are powered by a Radio Frequency (RF) power system by means of high power RF amplifiers and high voltage power supplies. The beam diagnostics and instrumentation present along the beam will provide all the necessary information to properly transport and accelerate the beam from the source to the Li loop target.

The Accelerator Facility also includes the Auxiliaries associated to the accelerator sub-systems: primary water cooling (except for specialized processes, as for the RFQ, where cooling system is associated to the RF cavity), vacuum system, gas supplies, electrical power,

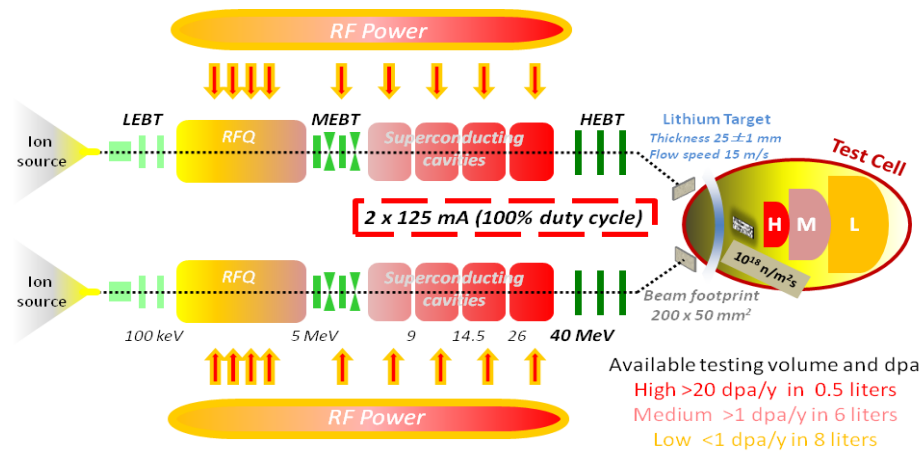


Figure 2.6: General IFMIF operation [3]

auxiliaries network (conventional electric distribution, compressed air) and local control systems.

### 2.3.5 The IFMIF-EVEDA Phase

As discussed in the introduction, IFMIF has unique features compared with other similar facilities worldwide. In Fig. 1.1 we can find a comparison of beam power in relation to energy. As shown, IFMIF beam power is above any other facility in relation to the same beam energy. Therefore, in order to validate this complex design, Engineering Validation and Engineering Design Activities (EVEDA) Phase were established in 2007 in the framework of the Bilateral Agreement between EU and Japan for the Broader Approach Agreement (BA) to Fusion.

The main objective of the EVEDA phase is: *to produce a detailed, complete, and fully integrated engineering design of IFMIF and all data necessary for future decisions on the construction, operation, exploitation and decommissioning of IFMIF and to validate continuous and stable operation of each IFMIF subsystem* [58].

As said, it is necessary to carry out several studies of system engineering and integration with detailed analysis of equipment specifications, safety generic analysis, etc., and on the other hand, it is necessary to validate the IFMIF installation concepts by building prototypes of its main units. Hence, three prototypes are being built in this phase:

- The low energy part of the accelerator (up to 9 MeV), tested at IFMIF current (125 mA) in continuous mode. Rokkasho, Japan. This is LIPAc, Linear IFMIF Prototype Accelerator, whose control system, design and development, is the target of this thesis. Throughout this work, LIPAc can be also named as IFMIF/EVEDA accelerator, which was its official name some months ago and it is still in use.
- The lithium target scaled-down third, including purification and monitoring systems planned for IFMIF, which will be tested in Oarai, Japan.

- The main components of high flow module, including 1:1 scale media and demonstration of thermal-hydraulic modules testing in Europe [59].

### 2.3.5.1 IFMIF vs LIPAc

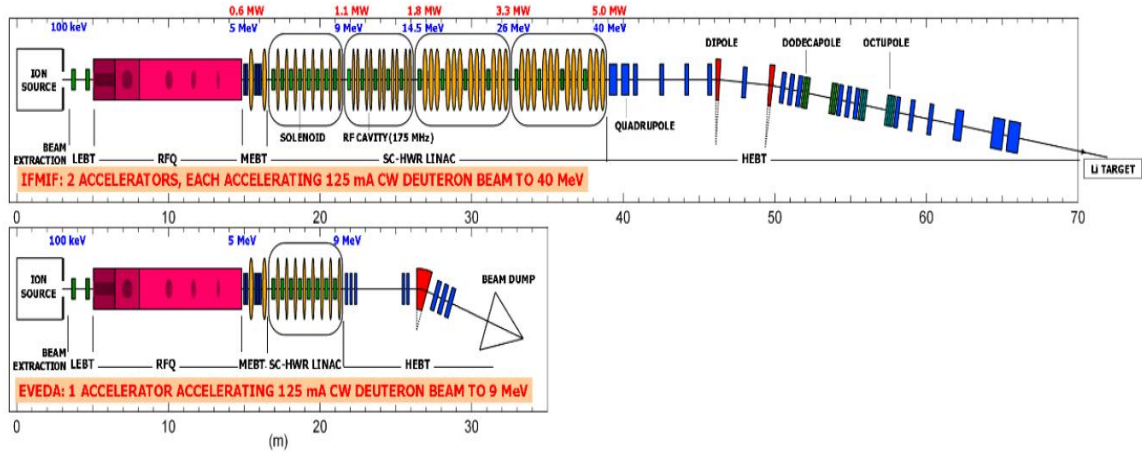


Figure 2.7: IFMIF beamline vs LIPAc beamline

As can be seen in Fig. 2.7, there is a complete correspondence between common units at both facilities, even LIPAc have a beam current of 125mA, which means up to 100% duty cycle. The difference between the final design and LIPAc is that in the prototype phase, the beam reaches only 9 MeV deuterons and subsequently detained in a BD designed for that purpose, not existing beam interaction with the target lithium, mission entrusted to IFMIF project. The equipment used in the prototype phase, up to 9 MeV, is identical to that for the IFMIF accelerator, consisting of an injector, an RFQ accelerator to 5 MeV and a cryomodule based on superconducting HWR cavity that provides a final energy of 9 MeV.

Space charge issues arise when working at low energy, 9MeV, with high beam current, 125mA and 1.125MW, see Fig. 1.1. These issues make LIPAc to have some very special requirements of magnets, cavities, diagnostic and safety which necessitates the design and implementation of a highly specialized control system that is developed in the framework of this thesis.

## 2.4 Summary

The greatest increase in demand for energy is envisaged to come from developing countries where, with rapid urbanization, large-scale electricity generation will be required. With environmental requirements for zero or low  $\text{CO}_2$  emission sources and the need to invest in a sustainable energy mix, new energy sources must be developed. Fusion could be available as a future energy option by the end of this century, and should be able to acquire a significant role in providing a sustainable, secure and safe solution to tackle european and global energy needs.

Europe has a large track record in fusion. Europe's JET (Joint European Torus) [60] located at Culham (UK) is the world's largest fusion facility and the only one currently capable of working with a Deuterium-Tritium fuel mixture.

Besides ITER, IFMIF is an essential facility in the World Fusion Programme as showed in the conclusion of the Fusion Fast Track Experts Meeting held on November 2001 [61]. Understanding the degradation of the mechanical properties of the materials critically exposed to  $14.1\text{ MeV } n$  fluxes, is a key parameter to allow accomplishment of the design and licensing a facility as DEMO.

Nowadays, fission and spallation sources are no relevant for fusion neutrons [62]. Hence, we can conclude IFMIF is a neutron sources tailor-designed to provide adequate flux, Fig. 2.3, and suitable energy to simulate the neutronic conditions in a fusion power plant.

The first challenge in the construction of IFMIF is to demonstrate its technical feasibility. For this, first steps have been taken through the design and development of a prototype, LIPAc, whose control system is described in this thesis.





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# 3

## Control systems architectures

*Nunca se ha de pensar en toda la calle de una vez, ¿entiendes? Sólo hay que pensar en el paso siguiente, en la inspiración siguiente, en la siguiente barrida. Nunca nada más que en el siguiente*

*Momo*, Michael Ende.

### 3.1 Introduction

One of the many definitions that can be found among the abundant literature on the control field, refers a control system as a manual or automatic mechanism used to manage dynamic processes by adjusting or maintaining physical variables such as temperature, speed, or flow rate. Basically, control consists of monitoring a parameter, detecting its changes and taking a proper action in consequence.

In recent years, control systems have assumed an increasingly significant role in the development and advancement of modern civilization and technology. Practically every aspect of our day-to-day activities is affected by some type of control system. A home-heating system, a refrigerator, an air-conditioner are all elements whose control system is their most relevant part. Control systems are crucial in modern industrial processes. Control systems are founded in all sectors of industry, such as quality control of manufactured products, automatic assembly line, space technology, transportation, power systems, robotics, and many others. Even such problems as inventory control, and socio-economic systems control may be approached from the theory of feedback control [63].

In control context, the system to be controlled is given various names: process, plant, and controlled system being perhaps the most common. In the so-called process industries (chemical, petroleum, steam power, fuel, etc.), one repeatedly faces the need to control temperature, flow rate, liquid-level in vessels, pressure, chemical composition, and so on; such applications are generally considered process control applications.

The functional specifications for control systems depend on its application. Three types of general purpose systems can be distinguished:

**Regulator systems.** The primary function of a regulator system is to keep a designated output within tolerances at a predetermined value despite the effects of load changes and other disturbances.

**Servo or positioning systems.** In a servo system or positioning control system the system is designed to modify the value of an output as demanded by a reference input signal, and in addition is required to act as a regulator system.

**Tracking systems.** In this case the reference signal is not predetermined but presents itself as a measured or observed signal to be tracked by an output [63].

Designing a control system is a creative process involving a number of choices and decisions. These choices depend on the properties of the system that is to be controlled and on the requirements that have to be satisfied by the controlled system. The decisions imply compromises between conflicting requirements.

When designing a control system, it is crucial to derive useful mathematical models of systems, signals and performance requirements. For the success of a control system design the depth of understanding of the dynamical properties of the system and the signals often is more important than the a priori qualifications of the particular design method. The models of systems considered in this work are in general linear and time-invariant. Sometimes they are the result of physical modeling extracted by application of first principles and basic laws. On other cases they follow from experimental or empirical modeling involving experimentation on a real plant or process, data gathering, they are based on the true experience. Some of the steps may need to be performed repeatedly. The reason is that they involve design decisions whose consequences only become clear at later steps, this is one of the major challenges when designing a control system. It may then be necessary or useful to revise an earlier decision. Thus, to design a control system is a process of gaining experience and understanding that leads to a proper balance between conflicting objectives and requirements [63].

Advances in computer technology [64], changes in the computer marketplace and demanding control requirements [65] have motivated control system software and hardware architectures development and fast evolution. The reduction in prices of powerful, user-friendly, networkable workstations coupled with the ever increasing cost and complexity of software stimulated new designs with a philosophy of control system evolution rather than totally new design, even on entirely new facilities [66]. This evolutionary design philosophy includes standardized structures and the use of open software standards to provide much greater flexibility to expand the size and automation of a system, to accommodate new high performance platforms, to reuse software developed previously, and to share software developed by other laboratories and industry. The recent and continuing efforts of standardization at all levels on protocols and other interfacing conventions means that equipments may be exchanged for newer versions, using entirely different internal technologies, which may then increase performance [67] or functionality of the entire control system. These changes have driven the designers of computer control systems toward a standardized modular architectures.

### 3.2 Control systems architectures in particle accelerators

The control system of a huge facility as a particle accelerator, must control the status and the operation of the machine, it could be considered the heart of the accelerator complex. The control system makes possible to have access to the different devices of the infrastructure from the computers located both locally and remotely. The status of the accelerator and

beam lines can be displayed worldwide via internet by monitoring the parameters of the control system. Accordingly, control system architectures can range from simple local control to highly redundant distributed control and they can be composed of one or more layers.

### 3.2.1 Local control architectures

Local control architectures characterizes systems in which sensors, transducers, controllers, and controlled equipment are physically close each other and the coverage of each controller is limited to a specific system or subsystem, see Fig. 3.1. Local controllers are typically capable of accepting inputs from a supervisory controller to start or terminate locally-controlled automatic sequences, or to adjust control setpoints, but the control action itself is determined in the local controller. Required operator interfaces and displays are also local. This configuration provides a significant advantage for the operator in order to solve machine issues, but requires the operator to walk around the facility to monitor and to note systems or respond to system incidents [4]. It is important to notice the difference between a system based on an unique local control architecture and a more complex control system such a distributed one, that meets several local control systems sharing information and working collaboratively, this is the case of LIPAc.

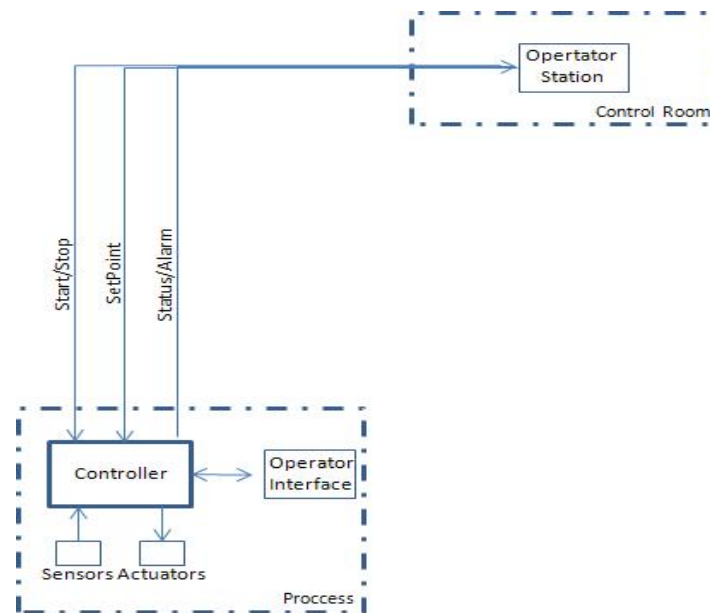


Figure 3.1: Local control system architecture [4]

### 3.2.2 Centralized architecture

Centralized control describes a system in which all sensors, actuators, and other equipment within the facility are connected to a single controller or group of controllers located in a common control room. Locating all controls, operator interfaces and indicators in a single control room improves operator knowledge of system conditions and speeds response to

kind of issue. This type of architecture was common for power plants and other facilities using single-loop controllers or early digital controls, but it has now been largely replaced by distributed control because of the high expenses associated with routing and installing all control system wiring to a central location. Centralized control systems should only be considered for not big facilities and if used, must have fully redundant processors. Where redundancy is provided in a centralized control system isolated wiring pathways must be provided to assure that control signals to and from equipment or systems that are redundant are not subject to common failure from the electrical grid, physical or environmental threats, Fig. 3.2 [4].

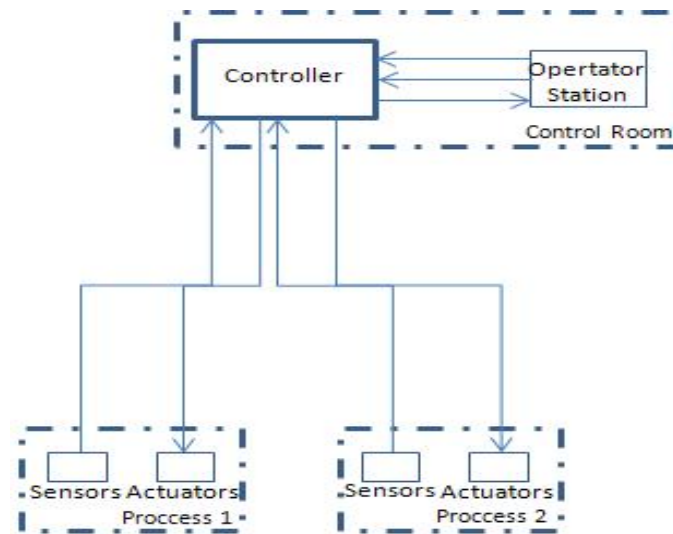


Figure 3.2: Centralized control system architecture [4]

A central processor unit coordinates all communications between the consoles and the lower level distributed processing power, and continuously updates a central memory which contains the whole machine status. This memory constitutes the machine database.

### 3.2.3 Distributed architecture

The idea of distributed system originates from the control implementation in process industry. This is where each physical element such as switches, pumps and valves are directly connected to its own control unit. The concept of distributed systems is to substitute a central controller with multiple controllers that control a particular part of the system. This means every single object or subsystem inside a system can potentially have its own control unit [68]. One problem with distributed process control used to be the realization of this implementation in industrial practice, where no proper design methodology and software tools had been developed until the achievement of EPICS which is explained in next chapter.

Distributed control system architecture, Fig. 3.3, offers the best features of both local control and centralized control. In a distributed control system, controllers are provided locally to systems or groups of equipment, but networked to one or more operator stations in a central location through a digital communication circuit. Control action for each system or

subsystem takes place in the local controller, but the central operator station has complete visibility of the status of all systems and the input and output data in each controller, as well as the ability to intervene in the control logic of the local controllers [4].

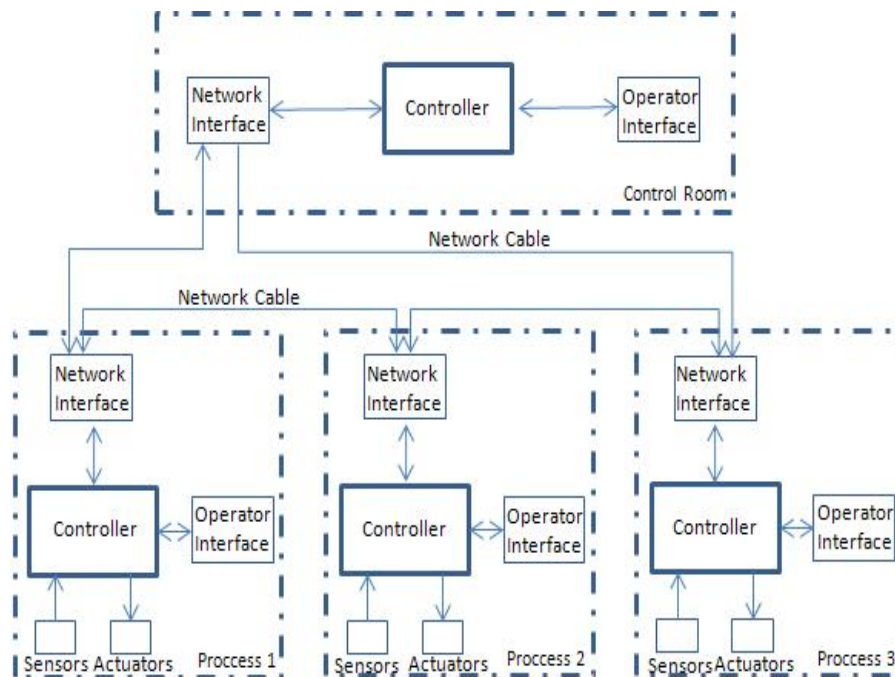


Figure 3.3: Distributed control system architecture [4]

There are a number of characteristics of distributed control architecture which enhance reliability:

- Input and output wiring are short and less exposed to physical disturbance or electromagnetic interference.
- An accidental breakdown in one area of the facility will not affect controllers in another area.
- Each local controller can function even with damaged communication with the central controller.

Following [4], there are also specific threats introduced by distributed control architecture that must be addressed in the design of the system:

- Interconnection of controllers in different locations can produce ground loop and voltage problems.
- If the central controller is provided with the ability to directly drive the output of local controllers for purposes of operator intervention, software malfunction in the central controller can influence multiple local controllers, endangering the system performance.

- Where redundant mechanical or electrical systems are provided, they should be provided with dedicated controllers, then, a failure of a single controller cannot affect more than one system.

S.K Singh [69], introduces the *generalized* distributed control system. Here, the aim is to provide a system where any required functionality can be carried out wherever spare capacity exists. The user has no interest in knowing where the computation is achieved as long as the result is properly provided. A distributed control system is different from the generalized distributed one since the hardware to be controlled is connected to specific computers. Thus, the part of the program must be executed at specific location. Usually, the field signals will be connected to the nearest node, in order to minimize the cabling efforts. Distributed control systems are more suitable for real systems, since the nodes reflect either a part or functional system of the machine. In distributed systems all drivers are able to transform the information themselves, without going through the central computer.

Following with the distributed architectures, different classifications can be set depending on the chosen criteria. For example, equipment distribution, it can be geometrical, systematic, functional or mixed.

In a **geometrical** distributed system, equipments are repeatedly located along the accelerator. The control nodes, distributed in each point, are capable of controlling a portion of the system. These nodes are identical in nature. The advantages of these systems are flexibility, ease of expansion and robustness, because if one of these nodes fails, the monitoring parameters may be carried out by those that continue functioning.

In a **systematic** distributed control system, devices are allocated and classified according to the different subsystems that compose the accelerator line, injector, low-energy beam transport..., etc.

In a **functional** distributed control system, nodes are positioned according to their functionality. Different nodes achieve different functions like timing system, alarm handling, fast data logging system..., etc.

It is important to note that several control systems are actually a mixture of two or even three of the above given visions. Depending on how we want to identify the roles of the different subsystems or devices, accelerator can be observed from either perspective. LIPAc mostly follows a systematic distributed control system. Each subsystem has a very specific role where controllers are provided locally but complete visibility of the system is carried out only in the central control, thus, full control and monitoring of the accelerator is achieved there. On the other hand, there is a local control system per each subsystem. Inside each local control system an example of functional control can be found, i.e., alarm handling, which reacts to a change in the thresholds of the values, regardless of the devices. An example of geometrical control can be found in the MPS, where equipments are repeatedly located along the accelerator in order to play the same function, to protect the machine in case of failure.

### 3.2.4 Single layer versus multilayer architecture

Beginning with single layer or monolithic architecture, where processing, data and the user interface all reside on the same system as a part of single software program, control systems have matured to multilayer architecture. Multilayer approach can fit further with local, centralized and distributed architectures. Single layer proposal can suit itself only in centralized and local architectures [69]. There are several appeals for single layer architectures which can be listed as given below:

- A single and centralized data store.
- Only one point access to the control system, eliminating any specialized access control.
- No possibility of data duplication.
- Easy for developers to maintain.
- Inherently fast and easily achievable time response.
- Lowered support base as there are fewer systems to support.
- System integration is easier as it is one system with a few external links.
- Management reporting is easier across systems as there is a single data store to pull data from.
- A single architecture and single developer framework and tool set.
- Easier for users to learn the system.
- Reliability can be achieved just by putting a duplicate system with simple logic.

But disadvantages could be more important than the advantages provided by these kind of systems:

- Indivisible systems are inappropriate to manage the complexity as any mistake will put the whole system down.
- As the operator interface is an integrated element of the system, it is directly exposed to any human mistake.
- Inseparable systems are unable to incremental development during machine commissioning and installation phase.

Several multilayer architectures consist of a personal computer as operator station, a local area network for data communications and front end micro-computers connected to the accelerator through signal conditioning and/or remote input/output interfaces. In a recent literature review, over three dozen systems world-wide were identified as employing this architectural model [64] [70], which is also known as *standard model*.

The operator interface provides a current view of the control process, historical data, alarm information, and a number of physics models to help maintain and predict the operation of the machine. The communication layer provides data transport between the distributed front-end computers and between the front-end and the operators. The front-end computers can provide distributed intelligence for data acquisition, data conversion, supervisory control, interlock management, closed-loop control and sequential control.

On the other hand, a multilayer architecture provides a more hierarchical control system. In a standard way, control systems can be partitioned in three layers: presentation layer (operator interface layer), application layer (server layer) and resource layer (equipment layer). The development presented in this work mostly follows a multilayer architecture.

A three layers standard model can be detailed as follows:

- Equipment layer is the lowest level of the control system which is directly interconnected to the accelerator equipments. This layer consists of the bins which host electronics modules which does the conversion between analog and digital data. Main kind of equipment that are presented in this layer are: VME, VXI, cPCI or smart instruments including electronics interface units and digital units as part of the instrument itself.
- Application layer provides different services to the other layers of control system. Major one can be remote booting and configuration of equipment layer devices, handling different operations between different equipment layer units. Application layer is also responsible of alarm monitoring, centralized interlock monitoring and data logging. It provides different services to operator interface unit.
- Operator interface unit is the layer which connects the accelerator with the operator and provides interaction with the machine. It consists of many displays and knobs for monitoring and controlling the accelerator status.

Field bus is the communication link between equipment layer nodes and sensors, actuators or complex front-end input/output devices to the local device servers. Examples are Profibus, RS 485, RS 422, Ethernet, GPIB, etc. High speed network provide communication architecture between application layer and presentation layer. Different choices are available, Ethernet, FDDI, Token ring, WLAN. Communication link and communication protocol are the basis of a multilayer system. As mentioned, depending on the interaction between the different layers of the system it can be categorized as centralized, local or distributed system.

### 3.3 Control systems architectures of other processes

Control system architectures may vary considerably between some sectors of technology to others. Besides control systems in particle accelerators, it has believed suitably to show, in a qualitative way, some control architectures in other areas of the technology developed in recent years.



### 3.3.1 A distributed architecture for a nuclear reactor control

A nuclear reactor produces and controls the release of energy from splitting the atoms of certain elements. In a nuclear power reactor, the energy released is used as heat to make steam to generate electricity. Control systems on many operating commercial nuclear reactors are obsolete, and increasing maintenance problems dictate conversion to computer-based systems. At present, several such digital systems have been qualified and installed. However, they trust on complex software and a centralized system architecture. A consequence of the centralized architecture is that a failure in a software function can cause a failure of the entire system even if the hardware is replicated [71].

To overcome these difficulties, there is the Extended Distributed Recovery Block (EDRB), see Fig. 3.4. It is a variation of the Recovery Block, a fault tolerant software structure first proposed by Prof. Brian Randell in 1975 [72], restated to include real time features, and restructured for distributed systems.

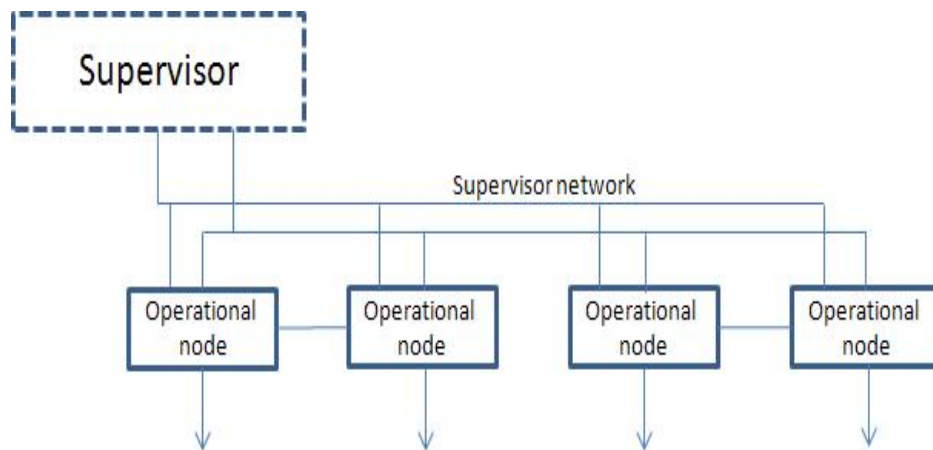


Figure 3.4: EDRB top level architecture

There are three types of computers (nodes) on an EDRB network:

- Operational: response for active control of the reactor and related systems.
- Supervisor: responsible for control of the network and the operational computers.
- Auxiliary: responsible for non-control functions such as maintaining the system data log.

Operational computers on the network are paired into active and shadow nodes. The active node executes a function, checks its result with an on-line assertion, and passes control to the shadow in the event of a failure. In the event of such a state, the supervisor node will recognize the problem from periodic status reports. It then sends an message to the operational nodes in order to restore consistency.

### 3.3.2 Control system architecture for TerraMax - The Offroad Intelligent Navigator

The challenge vehicle (TerraMax<sup>1</sup>) is based on an Oshkosh truck adjusted for drive-by-wire capability. The truck has six wheels, steering is accomplished with a servo motor turning the steering wheel, an actuator to move the brake pedal and direct electronic control of throttle and transmission [73].

In intelligent and real-time vehicles, control system architectures have been developed and changed into more sophisticated in the last few years. Hybrid architecture takes advantage of previous architectures, they constituted of two main levels:

- The deliberative routine level based on planning.
- A functional level based on reactive behavior.

These two levels together form the Situation Analysis and Logic (SAL) layer, it is also known as high-level intelligence [5].

Control and Execution (CE) layer, low level control, is in charge of speed regulation and path following. The truck is commanded in a closed loop given the trajectory and speed reference by the low level control, via a group of actuators and sensors. The separation of SAL and CE enable robust control and fast performance of the truck in presence of all kind of nonlinearities and delays in the mechanical system. This control architecture is shown in Fig. 3.5.

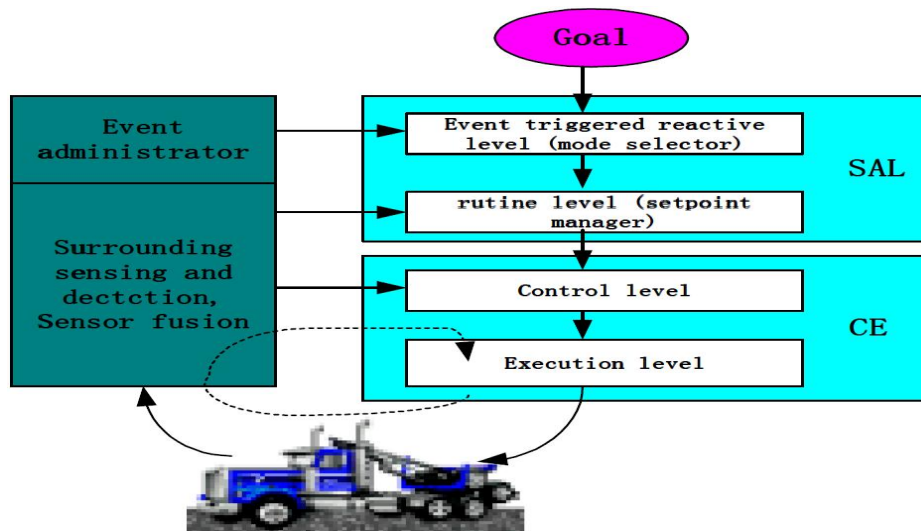


Figure 3.5: The general multi-level hybrid control architecture [5]

The TerraMax control logic consists of several of blocks. Some of these are continually active, some become active when they are called. The established structure allows separate

<sup>1</sup>Team TerraMax is an Oshkosh Truck Co. and Ohio State University partnership team with a technical alliance between OSU and University of Parma

and somewhat independent development. It also allows continual expansion of different and more complex cases and situation to be addressed during the development cycle.

### 3.3.3 A Satellite attitude control system architecture

Traditionally, satellite control has been ground operator intensive, requiring that most control operations be initiated from the ground. As the industry gains experience in satellite operations, it is possible to design more automation into satellite control systems [6].

In this section, it is described a new satellite attitude control system architecture, called the *Spacecraft Control System*. A raw version of this control system was scheduled to fly in 1997 onboard Indostar, a commercial geosynchronous communications satellite. The control system covers transfer orbit, acquisition and mission orbit modes. There are three distinct phases during which the Attitude Control System (ACS) must operate: transfer orbit, which begins when the satellite parts from the launch vehicle and during which the satellite must accomplish its mission orbit; acquisition, which is the process of locating the sun and the earth and aligning the satellite properly on station so its mission can be achieved; and mission orbit, during which the satellite must maintain its proper attitude and station. A block diagram of the entire control system architecture is shown in Fig. 3.6. The block diagram shows the interaction between sensors, control modules and the actuators. The processors for all of the sensors are: Horizon Sensors (HSA), Sun Sensors (SSA), gyros, Earth Sensors (ESA), and the Momentum Wheel Assembly (MWA) tachometer. The processed output from the sensors is used for error computation and input to the control systems: transfer orbit control, earth acquisition control, and mission orbit control. Then, the outputs of the control systems are distributed to the actuators: the Rocket Engine Assembly (REA), the momentum wheel motor, the magnetic torques, and the Electric Hydrazine Propellers (EHPs). The modularity of the system is intensified by separating error computation, control laws, and control distribution [6].

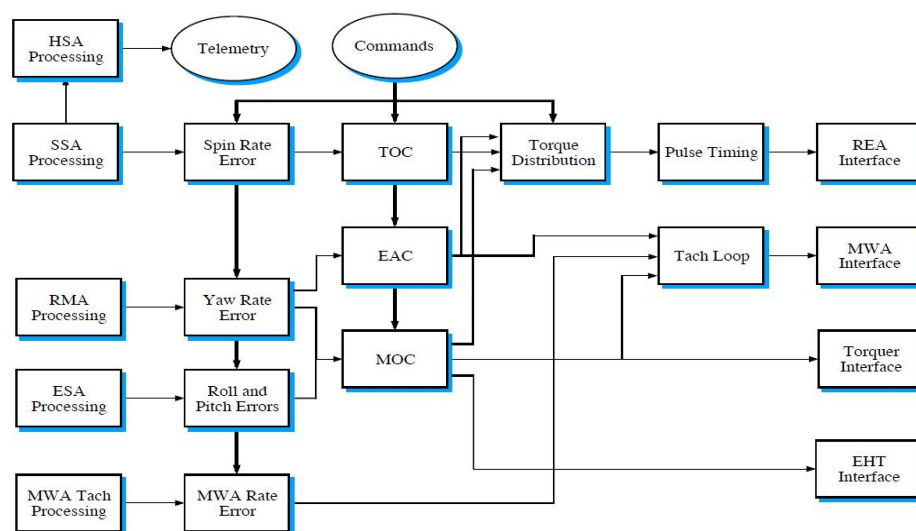


Figure 3.6: Satellite attitude control system architecture [6]

### 3.4 Summary

As accelerators increase in size and complexity, demands upon their control systems increase correspondingly. Particle accelerators difficulty is reflected in complexity of control system hardware and software. Same time imposing easy access and operation of the machine with higher degree of reliability and reconfigurability. Model-based procedures and fast feedback based upon even faster beam instrumentation are often required. Managing machine protection systems with hundreds or thousands of inputs is another significant difficulties. Increased use of hardware and software introduces new challenges of security and control [74].

In this chapter, a short control theory overview of continuous and discrete-time linear systems has been showed. In addition, a more extensive view about the different architectures that currently prevail in the control paradigm of large facilities, accelerators, has been explained.

The common denominator in all of showed questions in this chapter is:

- Given a control system: It must identify the system components and their function, including the comparator, controller, plant and sensor.
- Given a variable to be controlled: It must determine the structure of a system that will control that variable.
- Given a control system design problem: It must appreciate and understand that the complexity of most systems makes it difficult to predict their behavior.

Facing these issues can be done using one or more practical architectures explained above. It's not always easy to predict how a system will behave. Analysis tools are not perfect, and systems are not always completely understood.

In the case presented in this work, LIPAc control system, the prototype to control is properly understood, but the challenge is to meet the needs of the system, which, as discussed in previous sections, are beyond the intensity record of the present linac technology. It is also absolutely necessary to maintain uniformity in the contribution of each subsystem solutions. These requirements have led to propose a multilayer and distributed architecture for real-time control system in LIPAc.

Multilayer architecture in accelerator control is extremely adaptable to provide the needs of extensible machine and will fulfill the requirements of improvements and extensions in LIPAc. Innovative communication models and protocols will make the architecture more attractive.

There are a number of system design problems that are not optimally addressed by the standard model as defined above, and they can be considered as non standard models. Many of these issues can be addressed as extensions to the standard model however.

Fast changes in technology poses a big challenge for the control system as process control should use mature technologies. The most important thing is not using cutting-edge technology but the one which really works on real machines.

Ending with other scientific and technological fields, it is possible to observe that the role of the control systems in any technical development is crucial and essential. Control architectures can change notably depending on the processes or plants to control.



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# 4

## EPICS based control systems

*No tengo miedo a los ordenadores. A lo que tengo miedo es a la falta de ellos.*

Isaac Asimov.

### 4.1 Introduction

Fault tolerance and reliability are the most important goals to be achieved by the software of a control system. It should also provide mechanisms for machine diagnostics, which sometimes require intelligent data logging. Multiple operator interface and presentation units are always desired in an accelerator control system, in that case, proper care must be taken to avoid concurrent access to a single instrument or system from multiple nodes [69].

Therefore, the importance of using a correct software for the control development has become clear. Much of the work generated in this dissertation involves using an essential software tool in the elaboration of the control systems, namely EPICS. This chapter's primary mission is to explain what this tool is and place it in the context of particle accelerators.

To do this, first, the tool is presented in section 4.2, discussing the story of his birth, section 4.2.2, and the point at which it stands today, explaining its main properties beyond section 4.2.3. The next are some examples of its use in facilities similar to LIPAc which have been designed over an EPICS distributed control architecture, section 4.3.

Today, EPICS is not the only option when choosing software for the control system. Thus, alternatives to EPICS are showed in section 4.4. The chapters ends with a brief discussion in section 4.5.

### 4.2 Experimental Physics and Industrial Control System: EPICS

#### 4.2.1 What is EPICS?

EPICS is a set of open source software tools, libraries and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as a particle accelerators, telescopes and other large scientific experiments.

EPICS provides control and data acquisition for the experimental physics community. Because the capabilities required by the experimental physics community for control were not available through industry, the design and implementation of EPICS began. It also could be defined as a distributed process control system built on a software communication bus.

The functional subsystems, which provide data acquisition, supervisory control, closed loop control, archiving, and alarm management, greatly reduce the need for programming. Sequential control is provided through a sequential control language. Data analysis of the archived data is provided through an interactive tool. The timing system provides distributed synchronization for control and time marked data for data correlation across nodes in the network. The system is scalable from a single test station to a large distributed network with hundreds or thousands of channels. The functions provided to the physics applications have proven helpful to the experiments while greatly reducing the time to develop controls [64].

The basic components of a system running EPICS are:

- Operator Interface (OPI). This is a workstation which can run various EPICS tools.
- *Input/Output* Controller (IOC). Any platform that can support EPICS run time databases together with the other software components described in the manual. One example is a workstation. Another example is a *VME/VXI* based system using VxWorks or RTEMS as the real-time operating system.
- Local Area Network (LAN). This is the communication network which allows the IOCs and OPIs to communicate. EPICS provides a software component, Channel Access, which provides network transparent communication between a Channel Access client and an arbitrary number of Channel Access servers.

A control system implemented via EPICS has the physical structure shown in Fig. 4.1.

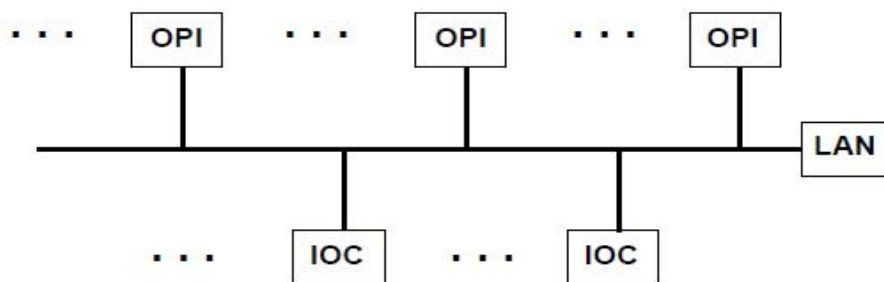


Figure 4.1: EPICS physical structure

#### 4.2.2 EPICS design history

EPICS was developed as a collaboration by a group with experience in control of various physics processes and industrial control. Three programs previous the EPICS development



were high order beam optics control, single shot laser physics research, and isotopic refinery process control. These systems were all developed between 1984 and 1987. The three programs embodied different aspects of data acquisition and control. The Ground Test Accelerator (GTAC) project, where EPICS development began as [75], required fully automated remote control in a flexible and extensible environment. The design group combined the best features of their experience, like distributed control, real-time front-end computers, interactive tools for monitoring and configuration, and workstation consoles, while taking advantage of the latest technology and the latest processors. Since the collaboration began, major steps have been made in portability between sites, extensibility in database and driver support. The EPICS name was adopted after the present multi-lab collaboration began[76].

Following [77] there are several reasons to attribute the success of EPICS:

**Technology:** One important factor inhibiting the copying of a control system is the rapid technological evolution of the components and techniques used. So when a few years pass after the successful commissioning of an accelerator and its control system, the components of that system out-of-date. With the sensible move toward standards by both the computer industry and the accelerator community, the use of standards instead of proprietary products or site-specific methods constitutes an obvious advantage.

**Specific Accelerator Requirements:** The different requirements of a new accelerator are often reasons for withstanding the installation of another accelerator's control system. However, the current tendency toward using similar control system methods and tools for all accelerators fights this argument.

**Knowledge of Software Internals:** One important reason to develop a control system is the need to have an intimate knowledge of the control system developed, since the developers are in charge of supporting the system throughout its lifetime.

**Unique Requirements:** Another reason that avoids commercial solutions is the unique set of requirements of each accelerator. Besides, no closed specifications are available at first and the system must be able to evolve to satisfy unspecifiable requirements.

### 4.2.3 Basic attributes

The basic attributes of EPICS are:

- **Tool Based:** EPICS provides a number of tools for creating a control system. This minimizes the need for custom coding and helps ensure uniform operator interfaces.
- **Distributed:** An arbitrary number of IOCs and OPIs can be supported. As long as the network is not saturated, no single bottle neck is present. A distributed system scales nicely. If a single IOC becomes saturated, its functions can be spread over several IOCs [78]. Rather than running all applications on a single host, the applications can be spread over many OPIs.
- **Event Driven:** The EPICS software components are all designed to be event driven to the maximum extent possible. For example, rather than having to poll IOCs for changes, a Channel Access client can request that it be notified when a change occurs. This design leads to efficient use of resources, as well as, quick response times.

- High Performance: Some scalable architectures can handle several thousand screen updates a second with each update resulting from a Channel Access event [79].

#### 4.2.4 Hardware-Software Platforms

EPICS core components (including IOC components) run on a wide range of systems. Currently this includes the following platforms, but new operating system platforms can be easily supported if they have reasonable support for sockets and threads. Currently most 32 bit processors are supported. Some limited testing has been performed on 64 bit processors.

Platforms that support EPICS operator interface (OPI) are Sun Solaris, Linux, Darwin, i.e. Mac OS 10 and Windows *NT/2000/XP/Vista* (32 bit). EPICS Local Area Network (LAN) supports most flavors of Ethernet and TCP/IP protocols via sockets API.

Regarding to Input/Output protocol (IOC) hardware supported, VME and VXI bus and crates, Various VME modules (ADCs, DAC, Binary *I/O*, etc.), Allen Bradley Scanner (Most AB *I/O* modules), GPIB devices, BITBUS devices: CAMAC and CANBUS, Motorola 68K, Intel x86, AMD Athelon, PowerPC, Sun SPARC and x86.

Finally, most of operating systems also support EPICS IOCs, VxWorks operating system, Real time kernel, Extensive *Unix like* libraries, RTEMS, Linux, Unix, Windows and Darwin.

#### 4.2.5 IOC Software Components

An IOC contains the EPICS supplied software components shown in Fig. 4.2

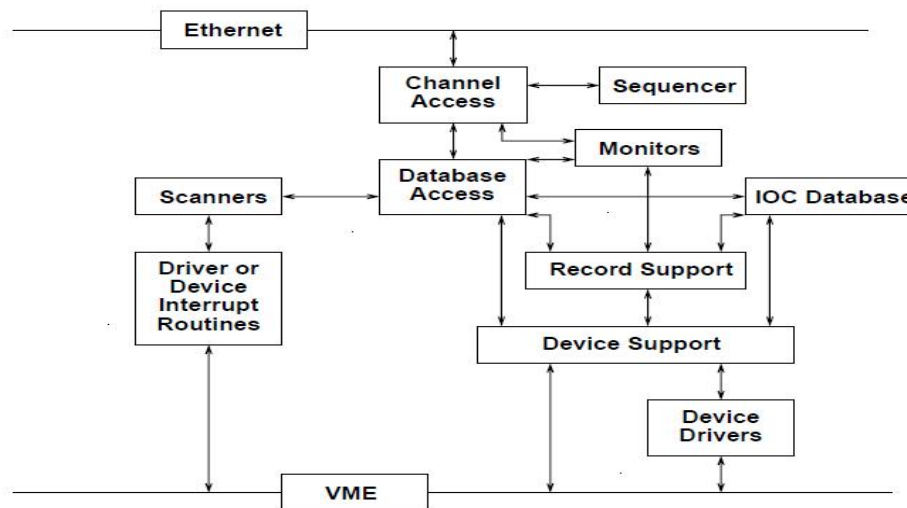


Figure 4.2: EPICS IOC components

- IOC Database: The memory resident database plus associated data structures. A database containing data structures is mainly a collection of records. A record is an

object with a unique name which behaviour is defined by its record type (class). Records have some controllable properties and an optional associated hardware.

- Database Access: Database access routines. With the exception of record and device support, all access to the database is via the database access routines.
- Scanners: The mechanism for deciding when records should be processed.
- Record Support: Each record type has an associated set of record support routines.
- Device Support: Device support is the means of providing functionality specific to access hardware. This is done by providing several functions which the record support layer will call when appropriate. The functions which must be provided depend on the record type being supported. Each record type can have one or more sets of device support routines.
- Device Drivers: A device driver is a specific computer program that operates or controls a particular type of device that is attached to a computer. A driver typically communicates with the device through the computer bus or communications subsystem to which the hardware connects. Device drivers access external devices. A driver may have an associated driver interrupt routine.
- Channel Access: The interface between the external world and the IOC. It provides a network independent interface to database access. Channel Access clients are programs that require access to Process Variables to carry out their purpose. A Process Variable (PV) is a named piece of data associated with the machine (i.e. readback, level, parameter, enable) with some attributes. In short, they are the basic data element in a network-based client/server EPICS architecture. Channel Access defines how PVs are transferred between a server and a client. The entire set of PVs establish a distributed real-time database of machine status, information and control parameters.
- Monitors: Database monitors are invoked when database field values change.
- Sequencer: A finite state machine.

#### 4.2.5.1 IOC Database

The heart of each IOC is a memory resident database together with various memory resident structures describing the contents of the database. EPICS supports a large and extensible set of record types, e.g. ai (Analog Input), ao (Analog Output), etc.

Each record type has a fixed set of fields. Some fields are common to all record types and others are specific to particular record types. Every record has a record name and every field has a field name. The first field of every database record holds the record name, which must be unique across all IOCs that are attached to the same TCP/IP subnet.

Data structures are provided so that the database can be accessed efficiently. Most software components, because they access the database via database access routines, do not need to be aware of these structures [79].

#### 4.2.5.2 Database Access

With the exception of record and device support, all access to the database is via the channel or database access routines.

#### 4.2.5.3 Database Scanning

Database scanning is the mechanism for deciding when to process a record. Five types of scanning are possible: Periodic, Event, I/O Event, Passive and Scan Once.

- Periodic: A request can be made to process a record periodically. A number of time intervals are supported.
- Event: Event scanning is based on the posting of an event by any IOC software component. The actual subroutine call is: *post\_event(event\_num)*
- I/O Event: The I/O event scanning system processes records based on external interrupts. An IOC device driver interrupt routine must be available to accept the external interrupts.
- Passive: Passive records are processed as a result of linked records being processed or as a result of external changes such as Channel Access puts.
- ScanOnce: The scanning system provides a routine scanOnce which arranges for a record to be processed one time.

#### 4.2.5.4 Record support, device support and device drivers

Database access needs no record-type specific knowledge, because each record-type has its associated record support module. Therefore, database access can support any number and type of records. Similarly, record support contains no device specific knowledge, giving each record type the ability to have any number of independent device support modules. If the method of accessing the piece of hardware is more complicated than what can be handled by device support, then a device driver can be developed.

Record types *not* associated with hardware do not have device support or device drivers.

The IOC software is designed so that the database access layer knows nothing about the record support layer other than how to call it. The record support layer in turn knows nothing about its device support layer other than how to call it. Similarly the only thing a device support layer knows about its associated driver is how to call it. This design allows a particular installation and even a particular IOC within an installation to choose a unique set of record types, device types, and drivers. The remainder of the IOC system software is unaffected.

Every record support module must provide a record processing routine to be called by the database scanners. Record processing consists of some combination of the following functions (particular records types may not need all functions):

- Input: Read inputs. Inputs can be obtained, via device support routines, from hardware, from other database records via database links, or from other IOCs via Channel Access links.
- Conversion: Conversion of raw input to engineering units or engineering units to raw output values.
- Output: Write outputs. Output can be directed, via device support routines, to hardware, to other database records via database links, or to other IOCs via Channel Access links.
- Raise Alarms: Check for and raise alarms.
- Monitor: Trigger monitors related to Channel Access callbacks.
- Link: Trigger processing of linked records.

#### 4.2.5.5 Database Monitors

Database monitors provide a callback mechanism for database value changes. This allows the caller to be notified when database values change without constantly polling the database. A mask can be set to specify value changes, alarm changes, and/or archival changes.

At the present time only Channel Access uses database monitors. No other software should use the database monitors. The monitor routines will not be described because they are of interest only to Channel Access [79].

#### 4.2.6 Channel Access

Channel access is a *software bus* that provides communication between various EPICS subsystems [80]. Channel Access provides network transparent access to IOC databases. It is based on a *client/server* model. Each IOC provides a Channel Access server which is willing to establish communication with an arbitrary number of clients. Channel Access client services are available on both OPIs and IOCs. A client can communicate with an arbitrary number of servers [81] [82] [83].

##### 4.2.6.1 Client Services

The basic Channel Access client services are:

- Search: Locate the IOCs containing selected process variables and establish communication with each one.
- Get: Get value plus additional optional information for a selected set of process variables.
- Put: Change the values of selected process variables.

- Add Event: Add a change of state callback. This is a request to have the server send information only when the associated process variable changes state. Any combination of the following state changes can be requested: change of value, change of alarm status *and/or* severity, and change of archival value.

In addition to requesting process variable values, any combination of the following additional information may be requested:

- Status: Alarm status and severity.
- Units: Engineering units for this process variable.
- Precision: Precision with which to display floating point numbers.
- Time: Time when the record was last processed.
- Enumerated: A set of ASCII strings defining the meaning of enumerated values.
- Graphics: High and low limits for producing graphs.
- Control: High and low control limits.
- Alarm: The alarm HIHI, HIGH, LOW, and LOLO values for the process variable.

Channel Access does not provide access to database records. This allows new record types to be added without shocking any software that accesses the database via Channel Access, and it allows a Channel Access client to communicate with multiple IOCs with differing sets of record types.

#### 4.2.6.2 Search Server

Channel Access provides an IOC resident server which waits for Channel Access search messages. These are generated when a Channel Access client (for example when an Operator Interface task starts) searches for the IOCs containing process variables the client uses. This server accepts all search messages, checks to see if any of the process variables are located in this IOC, and, if any are found, replies to the sender with an *I have it* message.

#### 4.2.6.3 Connection Request Server

Once the process variables have been located, the Channel Access client issues connection requests for each IOC containing process variables the client uses. The connection request server, in the IOC, accepts the request and establishes a connection to the client. Each connection is managed by two separate tasks: *ca\_get* and *ca\_put*. The *ca\_get* and *ca\_put* requests map to *dbGetField* and *dbPutField* database access requests. *ca\_add\_event* requests result in database monitors being established. Database access and/or record support routines trigger the monitors via a call to *db\_post\_event*.

#### 4.2.6.4 Connection Management

E. When a Channel Access server fails (e.g. its IOC crashes) the client is notified and when a client fails (e.g. its task crashes) the server is notified. When a client fails, the server breaks the connection. When a server crashes, the client automatically re-establishes communication when the server restarts.

### 4.2.7 OPI Tools

EPICS provides a number of OPI based tools. These can be divided into two groups based on whether or not they use Channel Access. Channel Access tools are real time tools, i.e. they are used to monitor and control IOCs.

#### 4.2.7.1 Examples of channel Access Tools

A large number of Channel Access tools have been developed. The following are some representative examples for the EPICS development used in LIPAc.

- EDM - Extensible Display Manager. The newest display manager/editor for EPICS.
- MEDM: Motif version of combined display manager and display editor.
- DM: Display Manager. Reads one or more display list files created by EDD, establishes communication with all necessary IOCs, establishes monitors on process variables, accepts operator control requests, and updates the display to reflect all changes.
- StripTool - General purpose stripchart tool.
- ALH: Alarm Handler. General purpose alarm handler driven by an alarm configuration file.
- AR: Archiver. General purpose tool to acquire and save data from IOCs.
- Sequencer: Runs in an IOC and emulates a finite state machine.
- BURT: Backup and Restore Tool. General purpose tool to save and restore Channel Access channels. The tool can be run via Unix commands or via a Graphical User Interface.
- PROBE: Allows the user to monitor and/or change a single process variable specified at run time.

#### 4.2.7.2 Examples of other OPI Tools

- VDCT - A Java based database configuration tool which is quickly becoming the recommended database configuration tool.

- JDCT: Java Database Configuration Tool. A JAVA based tool for creating run time databases.
- EDD: Display Editor. This tool is used to create a display list file for the Display Manager. A display list file contains a list of static, monitor, and control elements. Each monitor and control element has an associated process variable.
- SNC: State Notation Compiler. It generates a C program that represents the states for the IOC Sequencer tool.
- Database Tools - Tools are provided which generate C include files from menu and record type database definition files.
- Source/Release: EPICS provides a Source/Release mechanism for managing EPICS.

#### 4.2.8 EPICS Core Software

EPICS consists of a set of core software and a set of optional components. The core software, i.e. the components of EPICS without which EPICS would not work, are:

- Channel Access - Client and Server software
- IOC Database
- Scanners
- Monitors
- Database Definition Tools
- Source/Release

#### 4.2.9 Limitations of the current EPICS

EPICS represents a good platform to develop control systems with particular needs, but EPICS is far from being the end-all of control systems. It has attracted the attention because it represents a suitable toolkit upon which to build a variety of control systems tailored to particular needs, and the fact that the tool approach lends itself to collaborative development and progress. Being a LAN-based distributed system, it has no ability to attain the precision timing tasks required in all accelerators, an exception being its ability to time-stamp actions system-wide to the millisecond level using software and to the microsecond using available hardware tools. The solution to such a high-performance requirement has been to build the timing system external to EPICS and have EPICS manage it, distributing pulse delay and width data to specialized transmitters [77]. This approach using external timing systems sources based on VME bus is followed in LIPAc.



## 4.3 Examples of facilities using EPICS

### 4.3.1 ITER

ITER is based on the *tokamak* concept of magnetic confinement, in which the plasma is contained in a doughnut-shaped vacuum vessel. The fuel is a mixture of deuterium and tritium, two isotopes of hydrogen, it is heated to temperatures in excess of 150 million °C, forming a hot plasma. Strong magnetic fields are used to keep the plasma away from the walls; these are produced by superconducting coils surrounding the vessel, and by an electrical current driven through the plasma.

In order to control such a huge and technological machine, a global strategy called Control, Data Access and Communication (CODAC) system is developed. CODAC designates the central control system responsible for operating ITER. The different plant systems that constitute the ITER device will be driven by local instrumentation and control (I&C) designated as plant system I&C. The plant system I&C contains local controllers that are either PLCs or rack mounted computers controlling PCIe I/O and designated as *fast controllers*. Each plant system I&C also includes one Plant System Host (PSH), supplied by IO and implementing standard functions not requiring plant system specific software. During development and tests, the CODAC central infrastructure, that will include servers and operator workstations, is replaced with a computer designated as Mini-CODAC which implements a subset of the CODAC functions. The plant system I&C physical architecture is illustrated in Fig. 4.3.

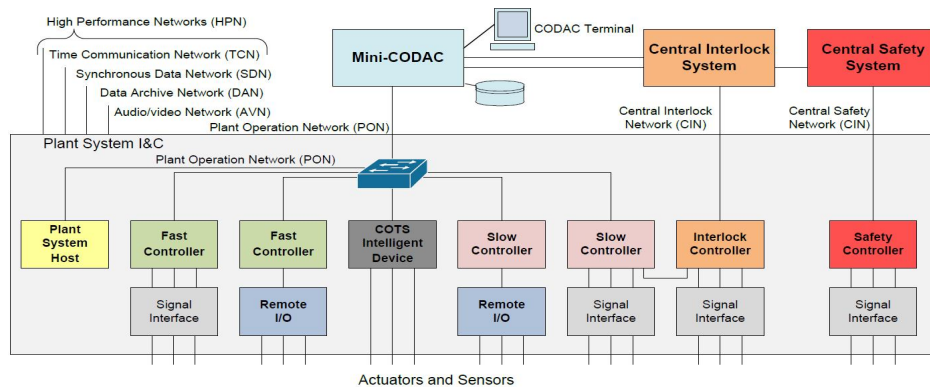


Figure 4.3: I&C Architecture before integration [7]

ITER control is conceptually designed following a clear separation between elements. The vertical tiers are control, interlock and safety, while the horizontal layers are the central control and the plant system control [84]. Thus, CODAC is the central control system responsible for operating ITER device. It is able to coordinate the operation of 161 plant systems. CODAC networks will connect to all these plant systems to central CODAC system [85], see Fig. 4.4. CODAC Core System is also serving as a reference for new EPICS developments in other scientific institutions [86].

EPICS is required for CODAC, Plant System Host (PSH) [87] and fast controllers [88]

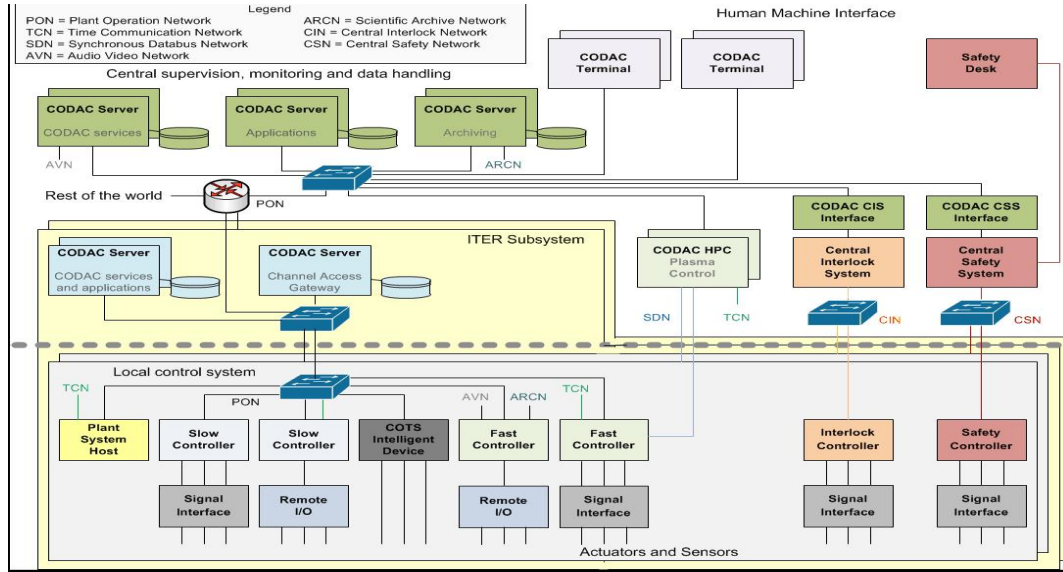


Figure 4.4: Physical architecture of ITER control system [7]

[89]. EPICS Channel Access is the standard communication protocol over the Plant Operation Network (PON), [90]. EPICS version for ITER includes:

- State Notation Language (SNL)
- Visual Database Configuration Tools (VDCT)
- An Autosave module.
- The standard EPICS IOC error logging.

#### 4.3.2 The Korea Superconducting Tokamak Advanced Research (KSTAR)

KSTAR is a long pulse, superconducting tokamak being designed to explore advanced tokamak regimes under steady state conditions. After the completion of the assembly in 2007, KSTAR (Korea Superconducting Tokamak Advanced Research) achieved the goal of first plasma in July 2008. During the commissioning period, the temperatures of the magnets were maintained below 4.5K, and all superconducting magnets were operated in the superconducting region. Plasmas of maximum current of 133kA and maximum pulse width of 865ms were obtained [91]. Thus, KSTAR Integrated Control System (KICS) has successfully fulfilled its missions of surveillance, device operation, machine protection interlock, and data acquisition and management.

The KICS, Fig. 4.5, is composed of the Central Control System (CCS), which provides the capability of performing supervisory control for the entire system and many local systems. The central control system contains the Plasma Control System (PCS), Machine Control System (MCS), Diagnostic Control System (DCS), time Synchronization System (TSS), and Interlock System (IS). These systems are connected by several network systems: the

machine control network-based on Ethernet, the Timing network-based on optical fibers with KSTAR's own timing network protocol, the reflective-memory-based real-time network (RTNet), and an interlock network based on optical ControlNetTM[92].

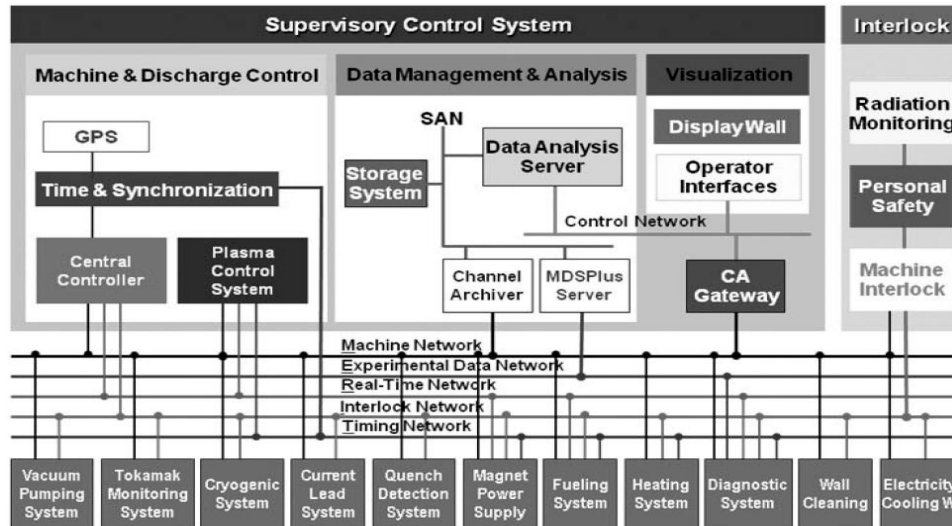


Figure 4.5: Structure of KSTAR integrated control system [8]

KICS integrates all subsystems controllers in a logically unified, single control system, controlling and supervising them remotely. By using EPICS, local control systems implemented in various platforms can be operated as if it were of the same type. Other substantial KICS requirements include supervision of the real-time feedback operation and 24 hour continuous plant operation. Central controller interfaced with the Plasma Control System (PCS) to monitor plasma current and position during the plasma discharge. KICS also includes both machine protection and personal safety interlock functionalities. For first-plasma operation, 11 types of diagnostic system were implemented. The main control room was constructed for remote operation and includes 22 operator consoles [8], [91]. Standardization of KICS control system is carrying out since 2010 [93].

#### 4.3.3 High Energy Accelerator Research Organization (KEK)

KEKB is the name of a particle accelerator used to study CP violation [94]. It is called a *B-factory* for its copious production of B-mesons which provide a mode to study and measure the CP violation due to its property of decaying into other lighter mesons. It is located at the High Energy Accelerator Research Organization in Tsukuba, Ibaraki Prefecture, Japan.

The control system is divided into three layers: presentation layer, equipment control layer and device interface layer, as shown in Fig. 4.6. The first two layers are divided functionally but connected with each other through a high-speed network such as FDDI. This is because the network traffic between the presentation layer and equipment control layer computers is expected to be dominant. The presentation layer which is composed of several workstations and about 6 to 10 X-terminals used as operator consoles. The functions which the workstations run can be executed by a UNIX server which has multiple processors. The

main network is an FDDI ring that has a node at each local control building. The equipment control layer consists of about 60 to 80 VME Input/Output Controllers (IOC) distributed around the KEKB rings. Each IOC will be allocated to a hardware group to avoid conflicts among groups or users. The final layer, the device interface layer, has standard modules such as CAMAC, GPIB, VXI, etc. There are special interface for controlling the magnet power supplies [95] and controllers and drivers for PLCs and WE7000 stations [96].

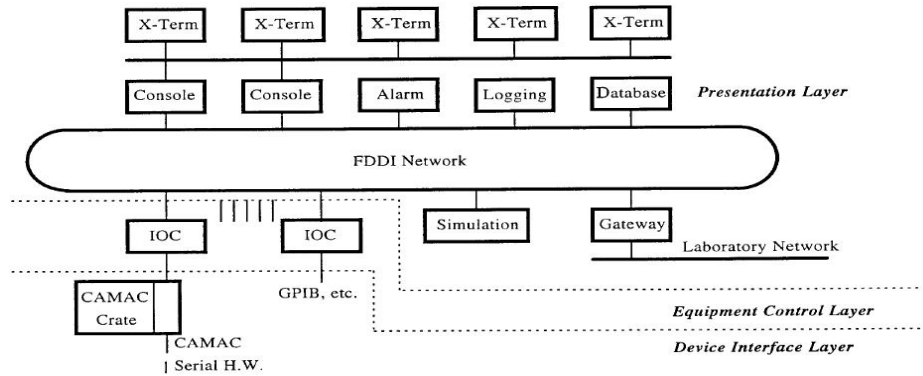


Figure 4.6: System architecture of KEKB Control System

#### 4.3.4 Japan Proton Accelerator Research Complex (J-PARC)

Japan Proton Accelerator Research Complex (J-PARC) is a 3-stage accelerator complex with a 200MeV Linac, a 3 GeV Rapid Cycling Synchrotron (RCS) and a 50GeV Main Ring synchrotron (MR). It is a large scale facility of the proton accelerator for the multi-purpose of scientific researches in Japan.

J-PARC control system has a three-layer, e.g. presentation layer, equipment control layer, and device interface layer as shown in Fig. 4.7. TCP/IP and UDP/IP network protocol were chosen besides the J-PARC standard field bus, in order to connect interface units that links accelerator component to the control system.

At the presentation layer, server workstations are used to make and run application programs for operations. This layer includes high-speed reliable network. The network is based on switched Gigabit Ethernet (GbE) operated in duplex mode.

At the equipment control layer, there are input/output controllers (IOCs) equipped with VME bus based computers with VxWorks and a large number of embedded computers running Linux or micro-iTRON (a Japanese real-time operating system for the embedded computer).

At the device interface layer, TCP/IP protocol is used on the 10/100 Mbps Ethernet as the common field bus. There is also a very large number of programmable logic controllers (PLC)<sup>1</sup> and intelligent equipment used in order to reduce cost and get flexibility. VME modules are used to obtain fast data acquisition and/or quick responses from micro-second to milli-second ranges [97].

<sup>1</sup>digital computer used for automation of electromechanical processes used in many industries and machines

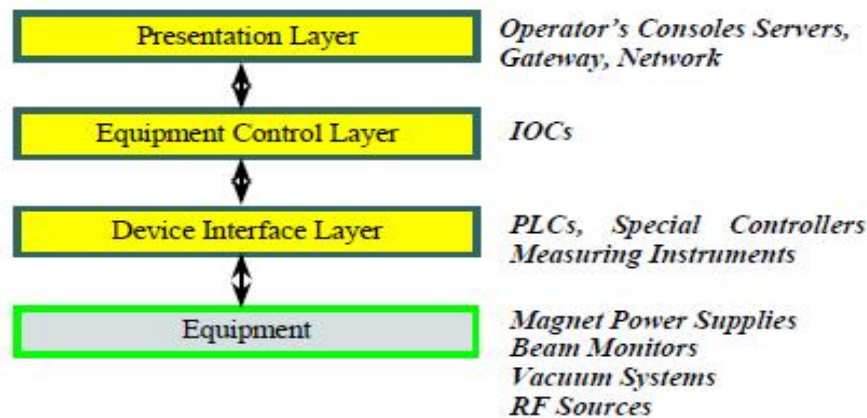


Figure 4.7: The standard model configuration of J-PARC Control System

#### 4.3.5 Diamond Light Source (DLS)

Diamond, a third generation 3GeV synchrotron light source[98], commenced operation in January 2007. The storage ring (SR) is based on a 24-cell double bend achromatic lattice of 561m circumference. It uses a full-energy booster synchrotron and a Linac for injection. The spectral output is optimized for high brightness up to 20keV from undulators and high flux up to 100keV. The current operational state includes seven photon beamlines, with a further fifteen beamlines [20].

For the accelerators and the initial 7 beamlines, the input output controllers (IOCs) are 267 VME VxWorks systems together with 202 Libera eBPMs running on ARM processors under Linux and 10 soft IOCs, running on PCs under Linux, all based on EPICS. The IOCs are structured by technical system and by geographical location and Linux PCs are used for all servers and operator interfaces. There are 1200 power supplies units (PSUs), all use the same digital PSU controller[99], eight variants of software and FPGA logic were carried out to suit different topologies. The EPICS interface to Libera eBPMs, was developed in-house, providing multiple data sets of high quality diagnostic data. Soft templates were used to build a model of the technical system by instantiating them with the full list of PVs. This gave a simulation of the control system with approx 350,000 PVs, served up by twelve MVME5500 IOCs [20].

#### 4.3.6 Spiral2

Spiral2 whose construction physically started by the beginning of 2011 at Ganil (Caen, France) will be a new radioactive ion beam facility to extend scientific knowledge in nuclear physics, astrophysics and interdisciplinary researches. The project consists of a high intensity multi-ion accelerator driver delivering beams to a high power production system to generate the radioactive ion beam being then post-accelerated and used within the existing Ganil complex. Spiral is the result of collaboration between several laboratories.

EPICS has been adopted as the standard framework for the control command system. At the lower level, pieces of equipment are handled through VME/VxWorks chassis or interfaced using the Modbus/TCP protocol; also, Siemens programmable logic controllers are coupled to the control system, being in charge of specific devices or hardware safety systems. The graphical user interface layer integrates both some standard EPICS client tools and specific high level applications. Relational databases are involved into the control system for equipment configuration, machine representation and configuration, CSS archivers and Irmis (mainly for process variable description). The first components of the Spiral2 control system are now used in operation within the context of the ion and deuteron sources test platforms [100].

#### 4.3.7 Keck Telescope

The W. M. Keck observatory operates the two 10m Keck optical / infrared telescopes on the summit of Mauna Kea, at an elevation of 4.145 meters. Keck 1 and Keck 2 have been operational since May 1993 and October 1996 respectively. A natural guide star (NGS) AO system has been scheduled on Keck 2 since Summer 1999, and the Keck Interferometer, a collaboration with JPL, was due to come on-line in 2002 [101].

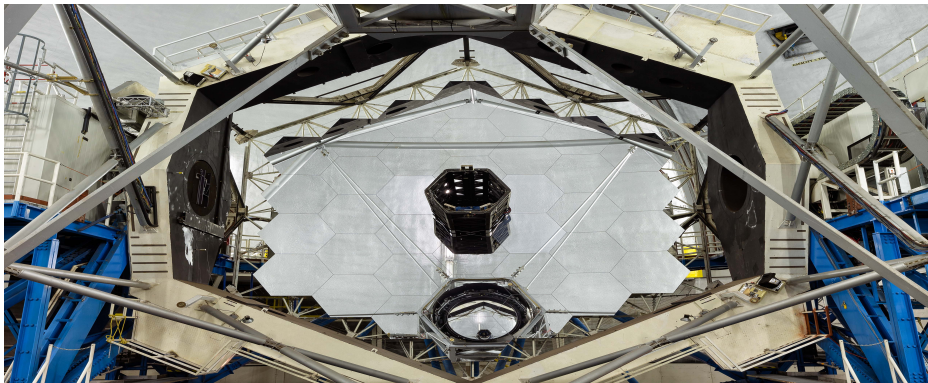


Figure 4.8: Keck 1 telescope, mirrors inside the dome. Courtesy of WMKO/Ethan Tweedie

The two 10m Keck telescopes run identical control systems, implemented using the Experimental Physics and Industrial Control System (EPICS). The new Adaptive Optics (AO) and Interferometer projects are also partly based on EPICS. However, other observatory subsystems, including acquisition and guiding, primary mirror control, and all the instruments, do not use EPICS. To manage this heterogeneous mix, the high level keyword-oriented Keck Task Library (KTL) was implemented. KTL can run on top of multiple message systems and allows a common API to be used for control, coordination and monitoring of all observatory subsystems [101].

## 4.4 Alternatives to EPICS

### 4.4.1 TANGO

Tango is an object oriented, multi language control system framework developed to fulfil the needs of control systems users. These needs are interfacing hardware in a reliable and performing manner, hiding its complexity, treating errors and alarms, distributing controls over the network, providing easy high level access, archiving long term data, user friendliness, interfacing some well-known commercial software and providing some kind of Web access. Tango became from a collaboration between institutes: *Alba-Cells*, *Anka*, *Desy*, *Elettra*, *ESRF*, *MAX-IV* and *Soleil* [102] [103].

The philosophy of Tango is to provide users with an object oriented control system which is powerful and easy to use. Tango uses CORBA [104] as network layer and offers the advantages of using CORBA hiding its details. Device is the basic TANGO component. It defines all the network features of equipment controlled with Tango and is defined within a single CORBA network interface. Therefore, from the control system client point of view, there is no difference between controlling sophisticated equipment like a RF cavity or a magnet cooling water flow meter [102].

### 4.4.2 DOOCS

The Distributed Object Oriented Control System (DOOCS), Fig. 4.9, was designed for the TESLA Test Facility (TTF) Linac. Currently it is extended to control the European X-Ray Laser Project (XFEL). It is completely written in C++ language and follows the object oriented programming paradigm since the design idea from the device level, including the device servers, up to the user display is based on objects. Recent developments for the client side applications are written in JAVA to allow them to be used on many computer platforms. This object oriented abstraction model helps for clean programming interfaces and in addition it helps in the overall system design including the hardware for a machine.

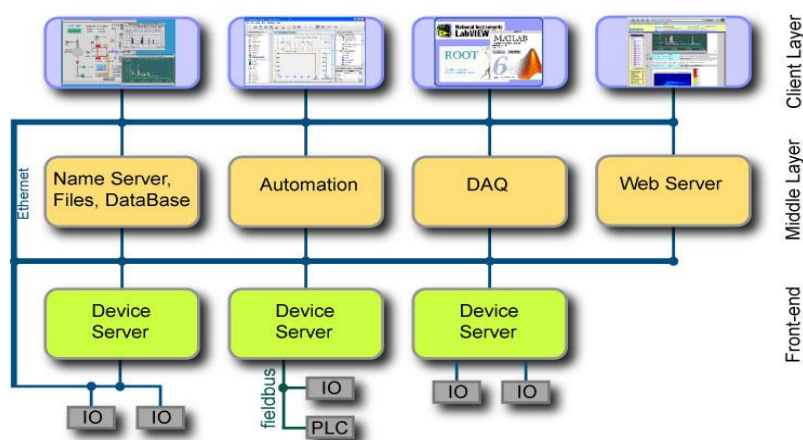


Figure 4.9: DOOCS Architecture

### 4.4.3 TINE

Historically, TINE is a spin-off of the ISOLDE Radioactive Ion Beam Facility Control System. Although originally PC-based it was soon ported to UNIX workstations. From the beginning it was designed to manage the needs of a large machine, namely HERA. With over 100,000 addressable control points and close to 200 device servers, HERA had to deal with issues of performance and scalability not usually seen in smaller machines. Although, HERA has been recently decommissioned, TINE has been shown to be a proper choice for smaller accelerator facilities, and will be the control system for the 3rd generation light source at PETRA3. In short, TINE is a mature control system featuring an efficient control system protocol, a large number of central services, a device access layer, and a large set of rapid application development tools for both client and server applications [105].

## 4.5 Critical comparison

Nowadays, the task of building a control system has been strongly affected by the ever increasing choice of Commodity-Off-The-Shelf (COTS) products. Many of the control problems have been solved and can be bought ready to use off-the-shelf. This has advantages in terms of price, functionality and development time. However, the products have to be integrated in order to behave as a unit. System integration is therefore one of the main tasks of a control system builder today [103]. In Fig. 4.10 a few control tool kits can be observed, but unfortunately, not all meet the fundamental requirements of integration and compatibility. EPICS is the option that covers more range, from the sensor to the interface. Today, EPICS is the overwhelming preference among accelerator facilities. Some of the options shown in the figure are obsolete or have only marginal developments that are not related to accelerator control systems.

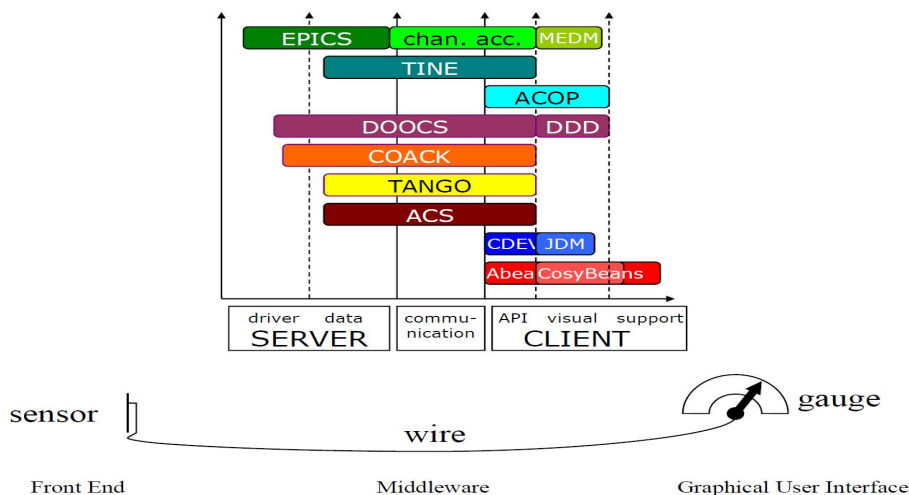
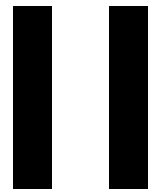


Figure 4.10: Fields covered by the various control tools, from the sensor to the GUI





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# **LIPAc Control System: Design and Development**



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# 5

## Linear IFMIF Prototype Accelerator (LIPAc) control system

*Les ocurre a muchos científicos, aunque no a todos: un día detienen su trabajo de investigación y se preguntan: ¿Qué es ciencia? ¿Cómo distinguir lo que es ciencia de lo que no lo es?*

*Yo, lo superfluo y el error, Jorge Wagensberg.*

### 5.1 Introduction

The control system of a facility as LIPAc must constantly ensure the status and the operation of the system. Thus, the control system is the heart of the facility and makes possible to have access to the different devices of the infrastructure, from the computers, located both local and central rooms, to the status of the building safety. The condition of the accelerator and its beam line can be displayed worldwide via internet by monitoring the parameters of the control system thanks to the EPICS Channel Access.

LIPAc control system is composed by five principal elements which will be precisely described in following sections: the accelerator Central Control System (CCS), the Local Area Network (LAN), the Personal Protection System (PPS), the Machine Protection System (MPS) and the Timing System (TS). In addition to these elements, there is a Local Control System (LCS) associated to each LIPAc subsystem. These thesis contributes to a greater or lesser extent, to all these elements.

Therefore, this second part of the document exposes the design and development of some elements of the LIPAc control system. This contribution meets the requirements set at the introduction, see section [1.1](#) and [1.2](#), which are faced again along the following sections. The work presented can be summarized in the following points:

- To define the control signals involved in the MPS.
- To interface and communicate the MPS with LCSs, LLRF control system and CCS.
- To define the control signals which are managed by some of the LCSs and the LLRF control system.

- To shape the necessary devices which are part of these LCSs and the LLRF control system.
- To interface these LCSs between themselves, LLRF control system and the CCS.
- To conceive the necessary architectures of each LCS and the LLRF control system.
- To transform control signals into processes variables (PVs), EPICS software.
- To develop EPICS based applications in order to meet the proposed architectures.

Regarding to this chapter, a LIPAc general overview is showed in 5.2, then its accelerator system is exposed in section 5.3. LIPAc control system is explained in section 5.4 which is comprised of CCS, LAN, TS, PPS and MPS. General concepts of LCSs are expounded in 5.4.6. The rest of the chapter encompasses the explanation of each LCS. Injector and Low Energy Beam Transport (LEBT) LCS in 5.5, Radio Frequency Quadrupole (RFQ) LCS in 5.6, Medium Energy Beam Transport (MEBT) LCS in 5.7, Superconducting Radio Frequency Linac (SRF) LCS in 5.8, High Energy Beam Transport (HEBT) LCS and Beam Dump (BD) LCS in 5.9, Radio Frequency (RF) LCS in 5.10 and Beam Instrumentation (BI) LCS in section 5.11.

## 5.2 LIPAc general overview

### 5.2.1 Overall description of the facility

LIPAc is a linear accelerator which is able of generate, accelerate and transport an intense deuteron beam in continuous wave mode; it corresponds to the low-energy part of the IFMIF accelerators, see section 2.3. Fig. 5.1 and Fig. 5.2 give an overview of the complete LIPAc facility and the accelerator vault. It will be assembled and operated at Rokkasho, in Aomori Prefecture, Japan.

LIPAc must demonstrate the feasibility of designing, building and operating a high current D<sup>+</sup> accelerator capable of continuous wave (CW) operation with the required availability. As the low-energy parts of the IFMIF accelerators are deemed to be the most critical ones, LIPAc is dedicated to study the accelerator sections up to 9 MeV (instead of 40 MeV for IFMIF) together with its auxiliaries and the associated infrastructure.

Consequently, the high-energy accelerating sections of IFMIF and its transport line designed for driving and shaping the beam toward the liquid Li target, are not tackled. Instead, a simplified transport line driving the beam to a beam dump is expected.

Main objectives for LIPAc to be experimentally investigated are:

- Produce a CW 125 mA D<sup>+</sup> beam with energy of 9 MeV (after the first SRF Linac cryomodule).
- Characterize the D<sup>+</sup> beam along the accelerator stages. This objective is fulfilled first in pulsed mode (with relevant pulse length) in order to alleviate the stress on components, to strongly reduce the activation level and possibly to permit the use of interceptive diagnostics

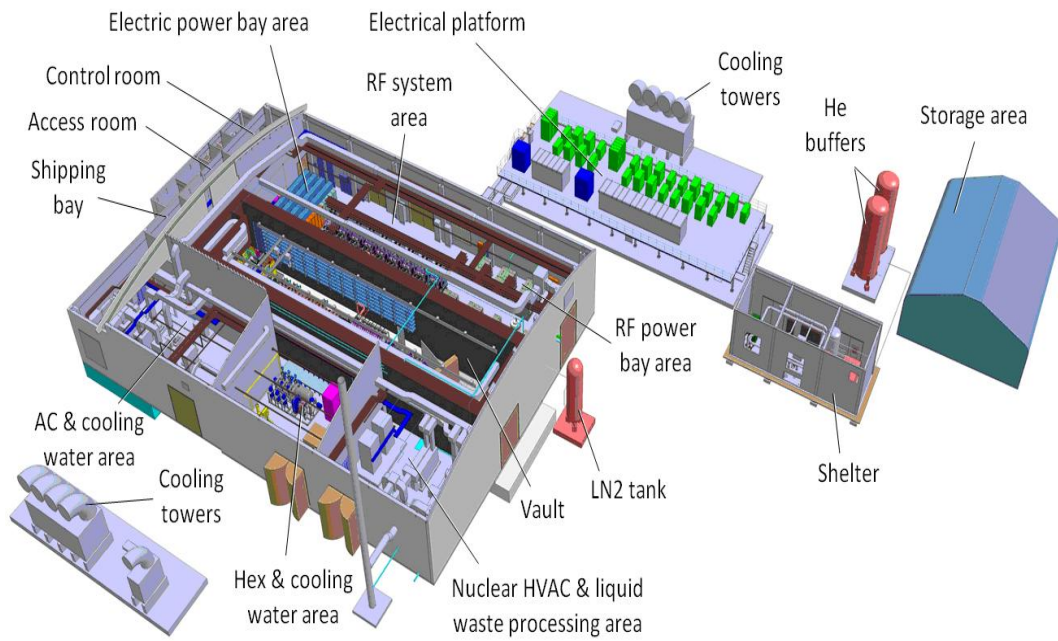


Figure 5.1: LIPAc facility 3D model

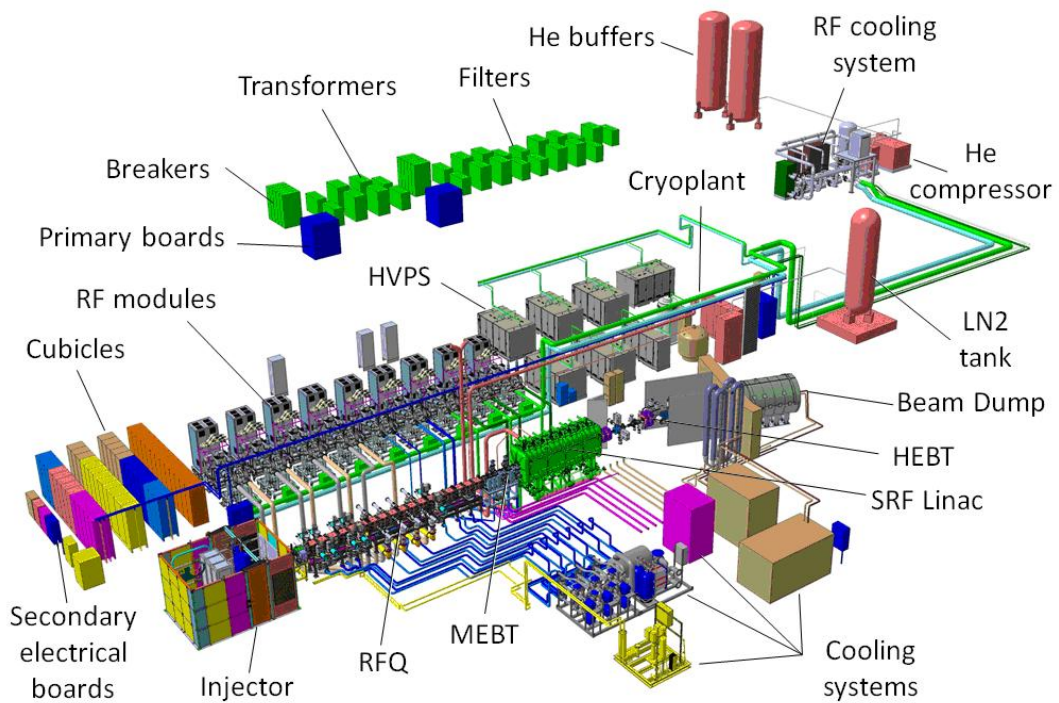


Figure 5.2: Accelerator 3D model [9]

### 5.3 LIPAc accelerator system

#### 5.3.1 Functional description of the acceleration process

LIPAc is composed of several subsystems whose functional unification process results in the generation, transmission, acceleration and beam stop, see LIPAc general layout in Fig. 5.3.

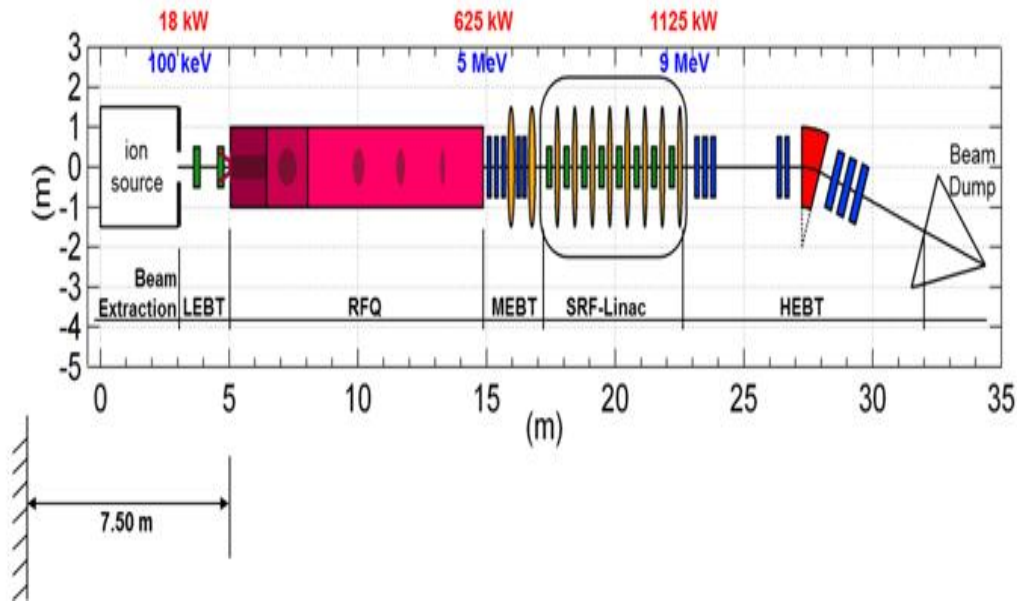


Figure 5.3: LIPAc general layout

Following Fig. 5.4, functional description of its subsystems is as follows. The beam of LIPAc is provided by an injector (2) using an electron cyclotron resonance (ECR) source (1). After being properly focused and filtered along the Low Energy Beam Transport (LEBT, 3), the D+ beam is accelerated by two successive systems: a normal conducting Radio Frequency Quadrupole (RFQ, 5) and a set of superconducting half-wave resonators (HWR) located within the Superconducting Radio Frequency Linac (SRF Linac, 7).

After controls and measurements of the beam parameters, the deuteron current is stopped into a Beam Dump (BD, 11, see Fig. 5.4). Between these systems, specific Medium Energy Beam Transport (MEBT, 6) and High Energy Beam Transport (HEBT, 9) lines transport and adapt the beam characteristics to the following structures.

Amplifiers chains, part of the Radio Frequency Power System (RF Power System, 4), based on tetrodes provide the RF power required.

A Cryoplant (8) is needed to cool down and maintain the near-zero temperature in the SRF Linac. The Beam Instrumentation (BI, 10) is distributed along the machine, besides the diagnostics included in each subsystem.

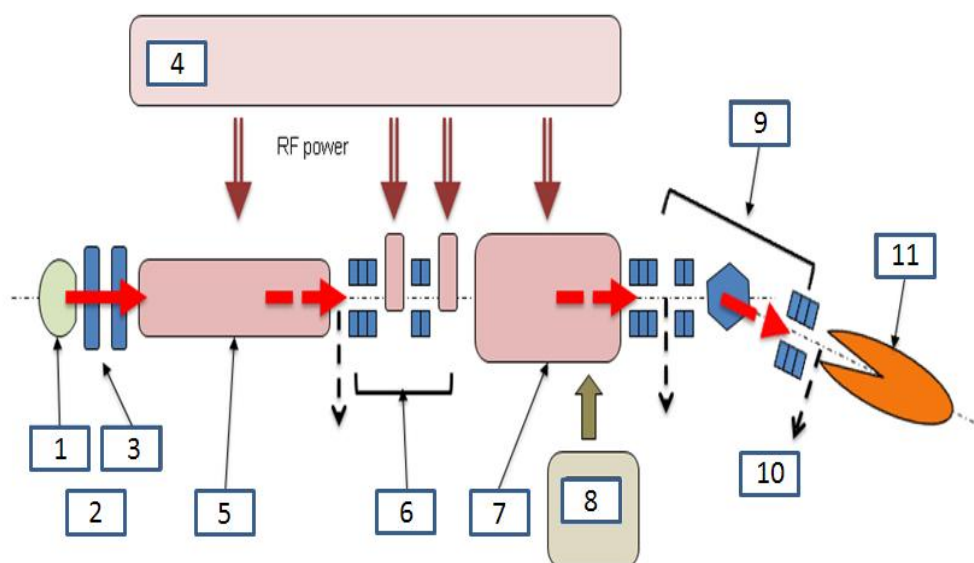


Figure 5.4: LIPAc general functional description

## 5.4 LIPAc control system

LIPAc control system consists of the remote control, monitoring and data acquisition of all devices, systems, subsystems and operations carried out in the accelerator vault. It uses EPICS as the main set of control software tools, providing the control with distribute and real-time features. This control system also manages the protection system of the machine and the protection system of the staff. As mentioned before, it is composed of five main elements, namely, accelerator Central Control System (CSS), Local Area Network (LAN), Personal Protection System (PPS) for not to expose to radiation doses, Machine Protection System (MPS) and Timing System (TS). Within each subsystem there is a Local Control System (LCS), which for this purpose, can be considered as a part of the overall control system and a very important part of the work described in this thesis.

Thanks to the EPICS Channel Access properties, all the process variables (PVs, see section 4.2.5) are available for each LCS and for the CCS. Only the central control system can take decisions at global level, since it is the only one who knows the full and overall accelerator status, see Fig. 5.5.

Main functional requirements of the LIPAc control system are the following:

- LIPAc control system must be able to remotely monitor and control operations of all the facility. This is the responsibility of CCS and LCSs.
- LIPAc control system should acquire all the data including control data and diagnostic data during the operation and archive and store these data. This is the responsibility of the CCS.

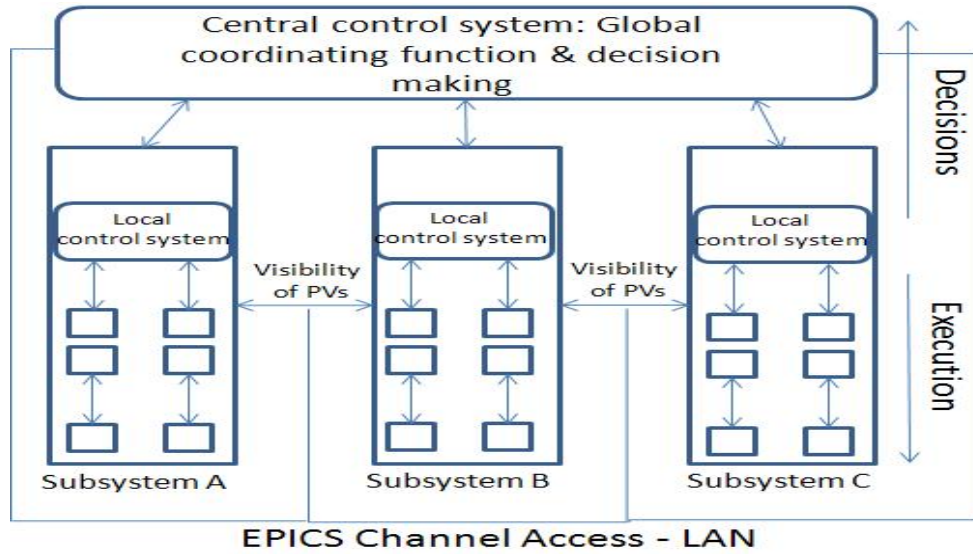


Figure 5.5: LIPAc distributed process control

- LIPAc control system should send the common timing signals to all the subsystems in order to synchronize clocks. This is the responsibility of TS.
- LIPAc control system should protect personnel from the radiation hazard produced by the high energy and high current deuterium beam from the accelerator operation. This is the responsibility of the PPS.
- LIPAc control system should protect the machine components from possible damages. This is the responsibility of the MPS.
- LIPAc control system provides the instrumentation common to all the plant control systems such as local area network and data buses. This is the responsibility of the LAN.
- LIPAc control system supplies the control and monitoring of each LIPAc subsystem. This is the responsibility of the LCSs.

LIPAc control system development is an unique and complex work due to the special characteristics of the prototype accelerator and its beam dynamics, that are, the unprecedented high beam intensity inducing the simultaneous combination of high beam power and high space charge, see 1.1. Therefore, control system development is related with general accelerator characteristics in the following way:

- LIPAc is aiming to produce a very powerful CW deuteron beam (1.1MW @ 9 MeV). The unavoidable beam losses along the accelerator, as well as the interaction of the beam with the beam dump, lead to an important rate of neutrons and  $\gamma$  radiations that must be properly controlled. On the other hand, the power of the beam itself could, in case of accidental or abnormal operation conditions, damage or destroy highly valuable



parts of the machine. The security and the safe operation of this facility rely on two independent protection systems, MPS and PPS, with different fast beam inhibition methods, their control must work with the greatest possible speed and assurance.

- To transmit energy from the RF system to the cavity and to drive properly the beam along the accelerator line, several subsystems are involved. Due to special characteristics of LIPAc, there is no previous experience in operating similar facilities. Thus, LCSs must allow the operators in the CCS to read and to modify parameters of the whole accelerator, i.e., main RF parameters, cavity diagnostics, magnets power supplies configuration, vacuum status, refrigeration, etc. LIPAc control system design justify the use of a common control strategy over EPICS, even if the devices involved are not ready for it. Restricted subnets will not exist but only one net where all parameters will be available.
- To achieve the RF system incremental power-up and to properly tune the accelerator cavities, LLRF control system must react as accurate as possible and must be able to provide all the necessary real-time information, both for manual and automatic functions.
- Beam losses must be observed and studied in order to fulfill beam stability in terms of transverse position and shape. To obtain this fundamental information several diagnostics devices have been installed along the accelerator line, these devices require an specific control and a fast data acquisition.

#### 5.4.1 Central Control System (CCS)

CCS satisfies the functions of central monitoring, central control, data acquisition and central archiving. The CCS monitors the operation of the entire LIPAc and controls the entire plant in accordance with the command given by the central operator and the local control systems status.

The CCS has common interfaces with the local control system of each subsystem. It can reach all the PVs running on the LAN by means of the EPICS Channel Access. CCS main element is the Operator Interface (OPI), see Fig 5.6, which provides the human machine interface environment necessary for monitoring and controlling the LIPAc plant via computer monitor displays. OPI consists of three layers:

- Global control OPI, used for overall accelerator operation
- Device group OPI, used for operation which is arranged in device groups
- Individual device OPI, used for start-up operation and detailed monitoring of each device.

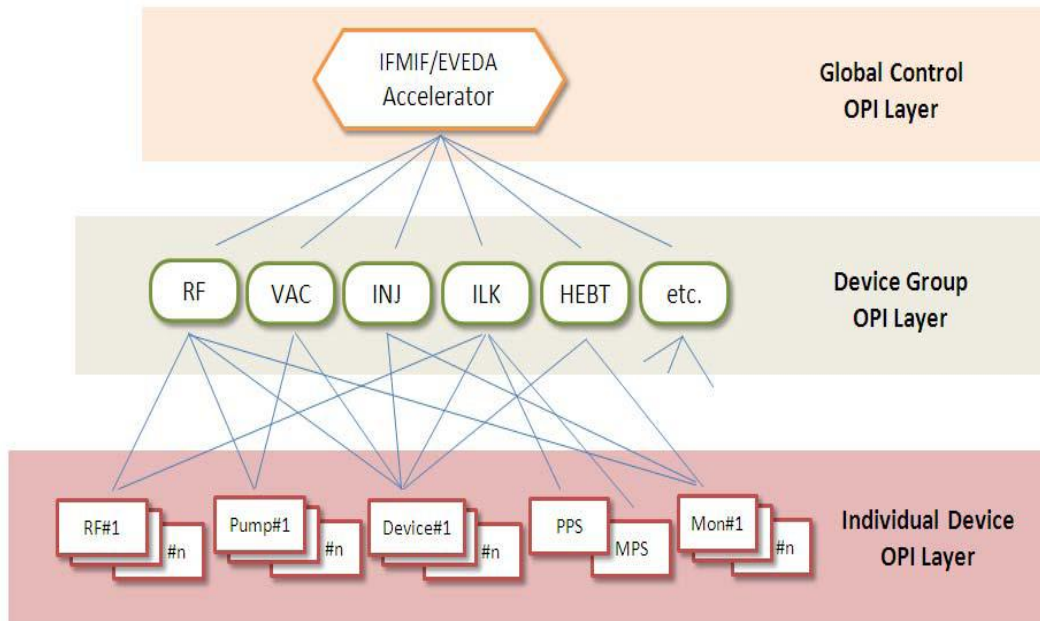


Figure 5.6: CCS operator interface layers

#### 5.4.1.1 CCS hardware configuration

CCS consists of Linux PCs, server and printer, see Fig 5.7.

- PCs for the global operation. Global control OPI and group control OPI run in 4 PCs.
- PC for LCS. Each device OPI runs in 8 PCs. (for Injector, RFQ, SRF linac, etc.)
- PC for data archive, logging of operation. This PC archives and logs the operation data.
- Server. Server supports the software platform and manages VxWorks environment and EPICS support
- Network printer. Graphs, data lists, etc.

#### 5.4.2 Local area network (LAN)

The Local Area Network (LAN) establishes the network connection between local control subsystems and CCS. The LAN system should be highly reliable and stable for secured transmission of the control signals and diagnostic data. For this purpose, the LAN system should have redundancies in the data path in order to cope with possible cable disconnections, poor connections or electric power faults. This LAN system adopts EAPS (Ethernet Automatic

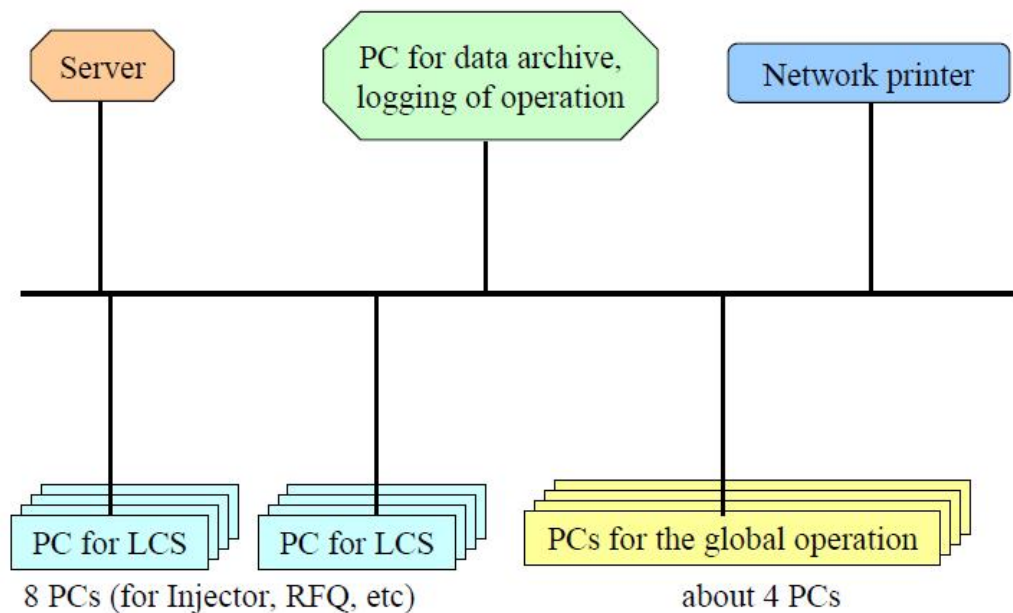


Figure 5.7: Elements of the CCS hardware configuration

Protection Switching <sup>1)</sup> which was identified as highly-reliable and efficiently redundant. If a failure of signal path takes place, EAPS reconfigures the data path in less than 1 sec by using a ring topology redundant protocol. The LAN system may consist of a center switch, edge switches and optical fibers among switches.

**Center switch.** Center switch is a core component of the LAN system. The center switch has some optical ports for connections with edge switches. It also has some metal ports for connections with the equipments.

**Edge switches.** The edge switches are interface switches for connections with the equipments. The edge switches have else some optical ports for connection with the center switch, and some other ports for connections with nearby equipments.

**Redundant electric power units.** Each center switch and edge switch have an emergency external power supply unit to maintain the functionality in case of the failure of the built-in power supply.

**Patch panels.** The optical fiber cables between the center switch and the edge switches are terminated at the patch panel of each switch, and connect to the optical connector. Between the optical port of the switch and the optical connector on the patch panel, an optical patch cord is used for connection.

<sup>1</sup>Ethernet Automatic Protection Switching (EAPS) is used to create a fault tolerant topology by configuring a primary and secondary path for each VLAN

### 5.4.3 Timing System (TS)

Control and data acquisition systems for accelerators need to ensure time-coherent in a distributed environment. This is usually carried out by a dedicated network whose purpose is to distribute a common notion of time from one master to many receiving nodes. Time distributed can be universal such as Coordinated Universal Time (UTC) or generated in the facility. Timing system is used not only to synchronize different processes but also to time-stamp and ensure coherency of the acquired data [106].

#### 5.4.3.1 TS hardware configuration

A timing system must ensure an accurate and uninterrupted operation, therefore it is VME (Versa Module European) based. J-PARC timing system configuration [107] has been successfully tested and it is VME based, LIPAc TS follows J-PARC hardware configuration [108].

LIPAc TS is configured mainly by a send module VME (Versa Module European), a receive module VME, a trigger generator and a gate generator. Send module has a master clock input, a reference trigger signal and a control signal. Master clock signal, reference trigger and control signal are sent to the receive modules. Then, the delayed signals are generated in complying with the control signal. Delayed signals are sent to trigger generator. Trigger generator and gate generator generate the electrical signals in complying with the delayed signals from the receive module, see Fig 5.8.

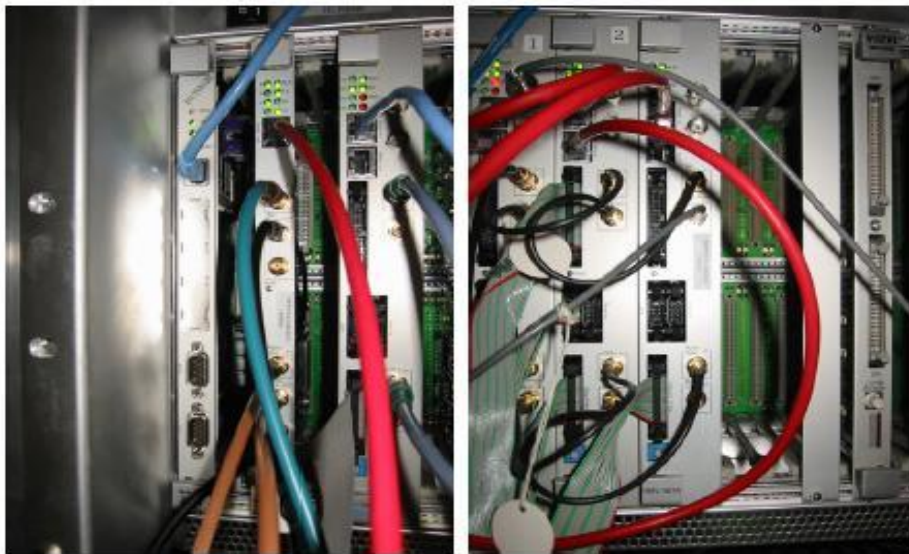


Figure 5.8: Send and receive timing system modules

### 5.4.3.2 TS module customization

LIPAc TS modules have been developed based on J-PARC TS modules [109]. In LIPAc, the counter is customized to adopt a 28bit counter (J-PARC is 24bit). On the other hand, the type bank is customized and increased substantially, J-PARC has 4 banks, LIPAc, 64 banks. Therefore, with this customization, a more efficient operation can be performed. The driver for LIPAc TS modules has been developed using EPICS.

### 5.4.4 Personal Protection System (PPS)

The PPS protects the personnel from the risk such as radio-active areas. For these purposes, the PPS manages entering and leaving the personnel into the radiation controlled areas in the LIPAc accelerator building. PPS is indispensable for safety management and licensing and it permits the accelerator operation only when there is no person in controlled areas [110]. It is based on the use of two programmable logic controllers (PLC), operating in parallel, see Fig 5.9. Each input status signal is transmitted to two PLCs independently. Both signals shall always be identical. On the output side, the PPS delivers always an authorization by two independent lines. Permission is given if and only if both lines are in the same state. All the interlock controllers and components are hardwired and fully redundant.

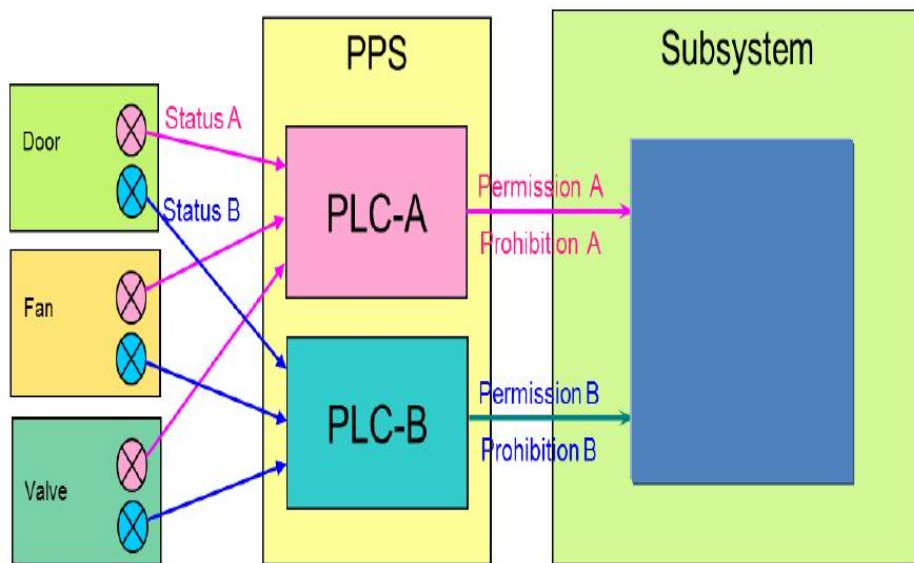


Figure 5.9: Principle of wiring for the PPS; all the links are directly hardwired

Functional requirements of the PPS:

- Beam operations of any system/component which generates radiation hazard are prohibited if there is someone in the controlled areas.
- During the operation of the beam or system/components which generates radiation hazard, any entry of the personnel into the PPS controlled area is prohibited.

- If someone enters into the PPS controlled area during the accelerator operation, the whole system should be immediately stopped.

The PPS consists of following components, see Fig 5.10:

- Operation Console
- Controller
- PPS internal equipments such as emergency stop switch button, door sensors, personnel entry monitoring system, and alarm devices.
- PC for monitoring of the signal status
- PC for control of cameras
- Monitoring cameras

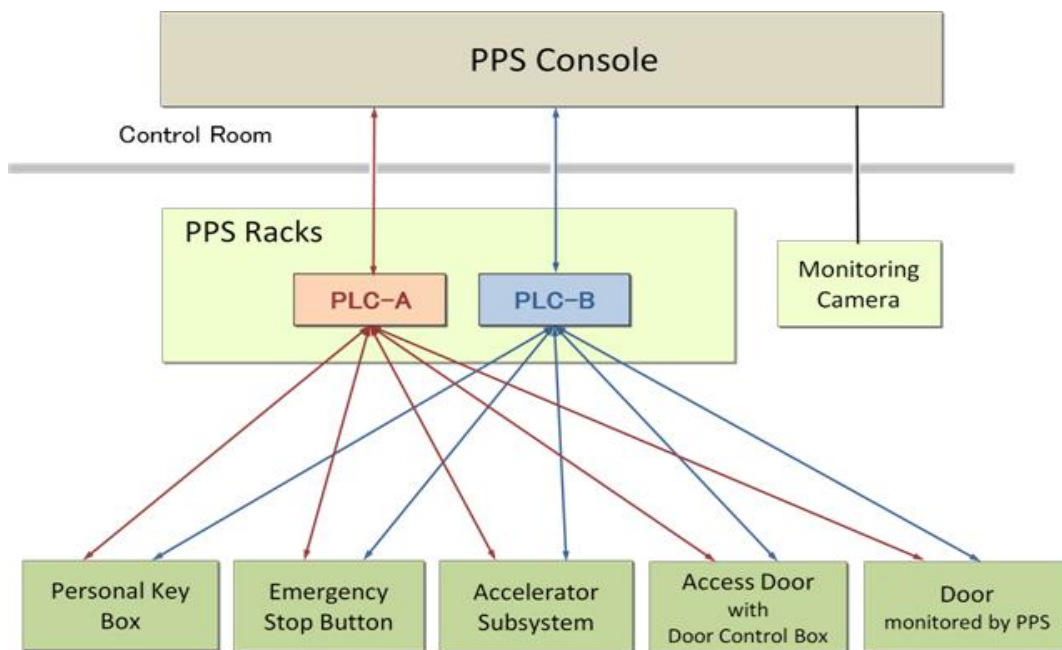


Figure 5.10: General configuration of PPS

The PPS is redundancy-based and developed using hard-wired signal paths independent of other systems. The PPS send the proper permission signals to accelerator subsystems. Each accelerator subsystem must establish a certain interlock to operate only when the permission signal is active. If the PPS cancels (resets) permission signals, each subsystem must safety and immediately stop the equipment, communication between PPS and subsystems is detailed in Fig. 5.11.

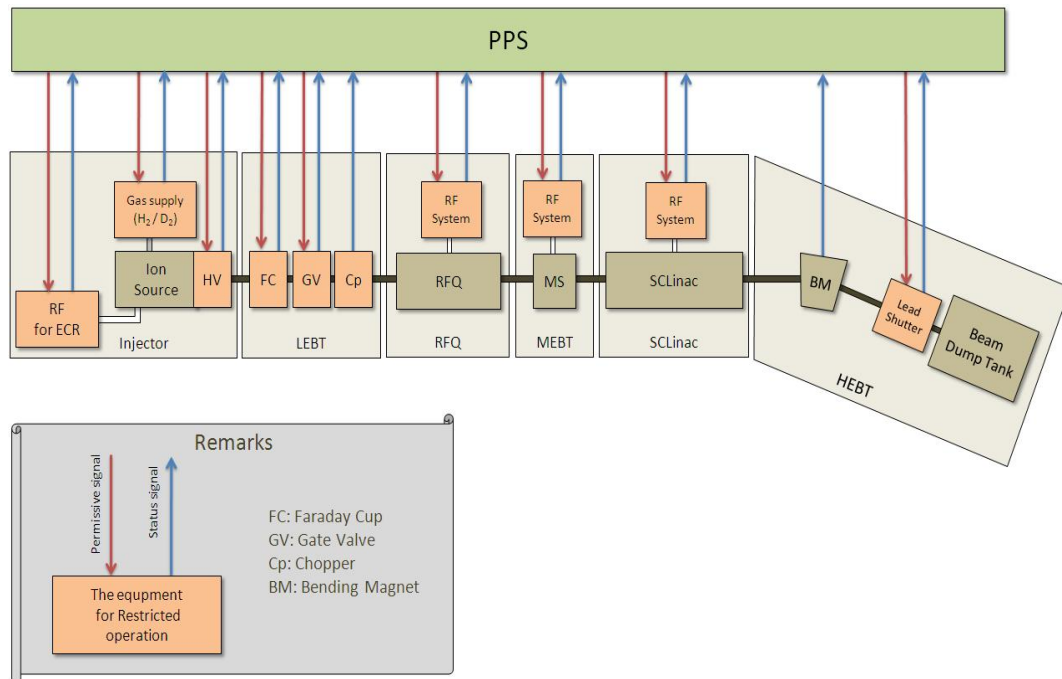


Figure 5.11: Overview of the PPS and subsystems communication

### 5.4.5 Machine Protection System (MPS)

Due to the use of a high-intensity D<sup>+</sup> beam, some operation failures cause severe beam bombardment on the accelerator surface, which results in both mechanical damages and the activation of the accelerator components. In order to avoid this undesirable situation, the beam should be cut off immediately after detection of a failure.

The purpose of the MPS system is to protect the accelerator (beam pipes, cavities, beam dump...) from any damage that could occur, due to the malfunctioning of a component or due to the mistuning/misalignment of the beam. The MPS input signals can be any relevant status signals coming from the subsystems like vacuum, temperature, cooling, RF, LLRF, PLC, low voltage power supplies, valves, slits, focalization, arcing, quench, cavity field, tetrodes status, beam loss monitor (BLoM) or interceptive diagnostics among others. MPS outputs are stopping the beam (reset, fast, slow) and closing the valves, see Fig 5.12.

Within the MPS, there are different ways of cutting off the accelerator operation, following different protocols, depending on the devices involved and the severity of failure in the system, these beam inhibition methods are shown in Fig. 5.13 and explained below. All of these methods are encourage to work in very low response times, therefore, MPS emergency stops are carried out at hardware level. EPICS software processing is only used to inform the operator in real time.

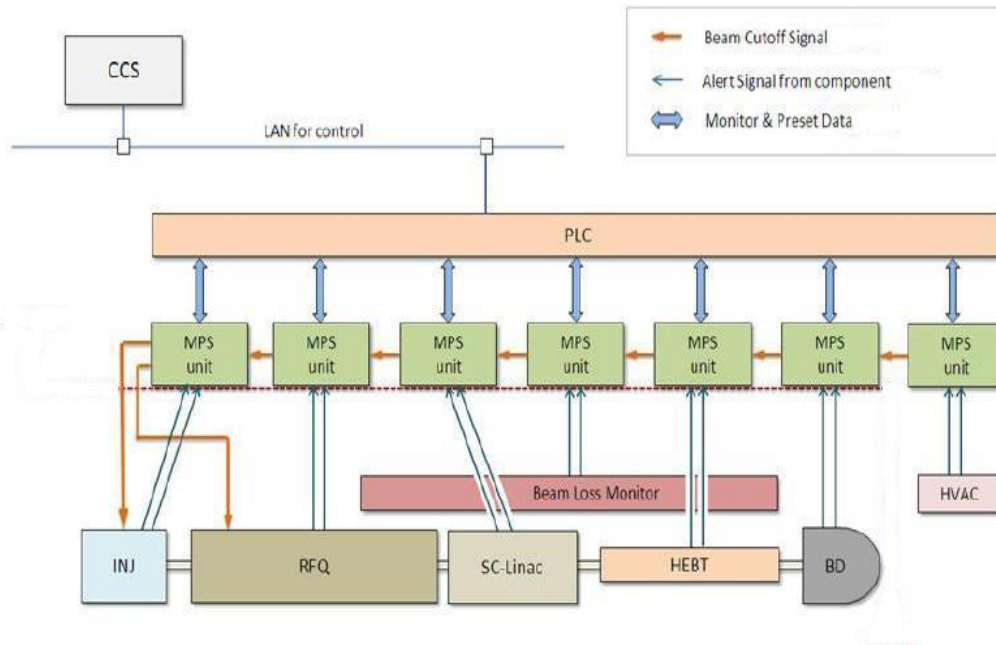


Figure 5.12: Principle of the LIPAc MPS system

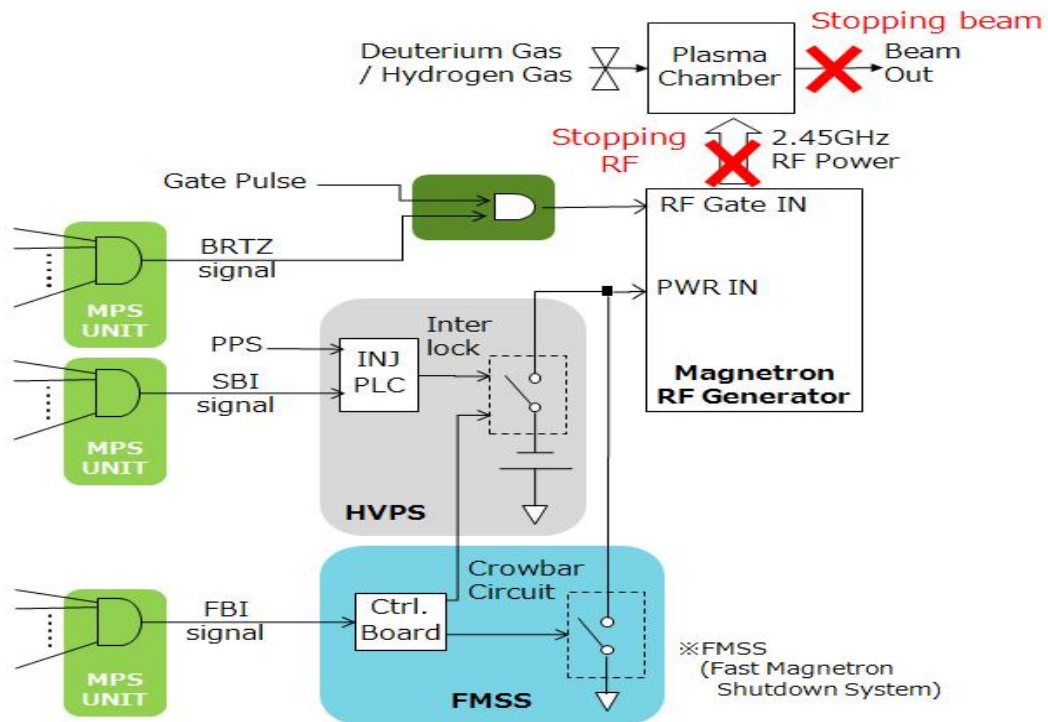


Figure 5.13: MPS beam inhibition methods

**Beam reset to 0 ( $< 50\mu\text{s}$ ) BRTZ.** Stopping the beam at source level will be available only in pulsed mode and low duty cycle. The principle is, on MPS request, to reset to 0



the beam pulse as fast as possible by resetting the signal sent to the electron cyclotron resonance (ECR) source, RF modulator. By this way, the duration of the selected beam pulse is shortened but the next pulses are again permitted as soon as the MPS line is back to normal state. The delay between the MPS request and the actual stop of the beam should be shorter than  $50\ \mu\text{s}$ . Such a way of stopping the beam will be very useful during the optimization phases especially when using automatic computer-assisted tuning procedures, Fig 5.14.

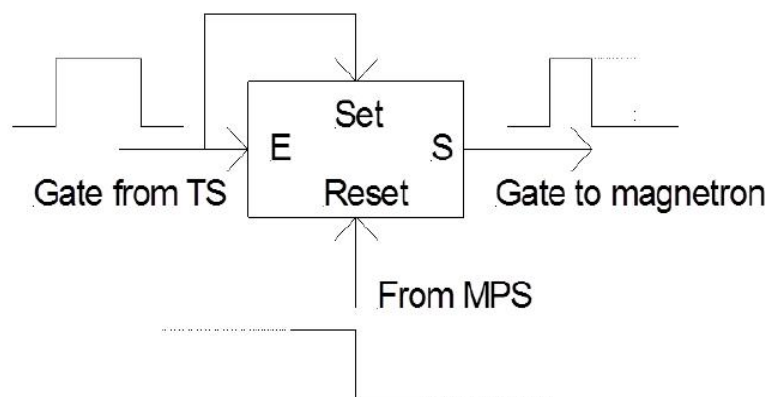


Figure 5.14: Beam reset scheme

**Fast beam inhibition ( $< 20\mu\text{s}$ ) FBI.** The beam is stopped still at the source level, but in this case, by activating a *crowbar* system implemented on the high voltage power supply of the RF magnetron. The fast beam inhibition will be always activated during CW or high duty cycle operation and also each time the fault having caused this stop requires a long duration procedure for curing (vacuum, water cooling...). It is considered as a safer way to stop the beam than the beam reset. Specific actions will have to be done at control system level in order to reactivate the system.

**Slow beam inhibition ( $\approx 300\text{ ms}$ ) SBI.** The beam is stopped by opening the breaker of the magnetron HVPS without using the crowbar discharge. The RF power in the source and thus the beam current are decreasing slowly. The beam is stopped after about 300 ms. The slow beam inhibition will be used in several cases when a fast beam interruption is not required (temperature alarm, BLoM electronics or HVPS fault). As for the fast beam inhibition, specific actions will have to be done at control system level in order to reactivate the system.

#### 5.4.5.1 Valves management in the MPS

In case of vacuum fault on the accelerator, all the sectional valves will be closed together and at the same time, the beam will be stopped by the fast inhibition circuit, Fig 5.15. Within each LCS other possible measures may be taken

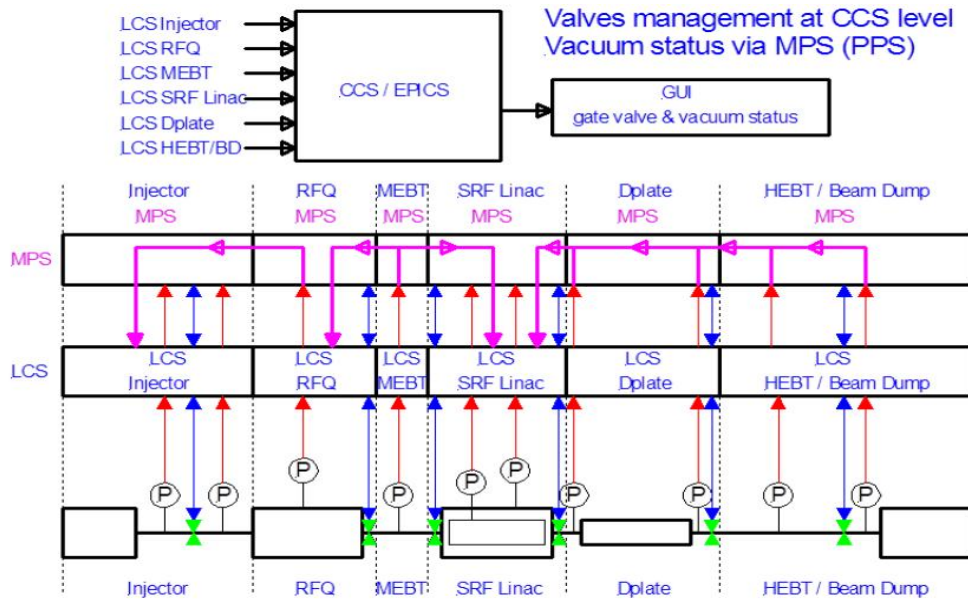


Figure 5.15: Interconnection between LCS and the MPS chain

#### 5.4.6 LIPAc Local Control Systems (LCSs)

##### 5.4.6.1 LCSs general architecture

As mentioned before, a local control system in LIPAc refers to each of the control systems, autonomous and independent, which control each accelerator subsystem, see section 5.3.1:

- Injector LCS
- MEBT LCS
- RFQ LCS
- SRF linac LCS
- RF LCS
- HEBT and BD LCS
- BI LCS

The main function of the LCSs is, obviously, to control its own subsystem, displaying their own PVs for the rest of LCSs and enabling access and modification of these PVs by the CSS. To implement this architecture, local control systems shall be based on EPICS.

LCSs are composed of different elements but following the organization shown on Fig. 5.16, a three layers architecture. The lower level consists of equipment (power supplies, diagnostics, sensors, motors) connected to the intermediate level via specialized links. The middle layer consists of EPICS front-end systems (so-called input-output controllers (IOCs)). The upper layer, part of the CCS, consists of workstations, which either play dedicated roles (file server, archiver) or offer a man-machine interface function. These two levels communicate through TCP-IP on Ethernet.

On the other hand, the software interfaces between the different LCSs should be compatible in order to fulfill the needs of data communication between the LCSs themselves and between the LCSs and the central supervision. This homogeneity at the level of software is guaranteed by the general use of the EPICS tools.

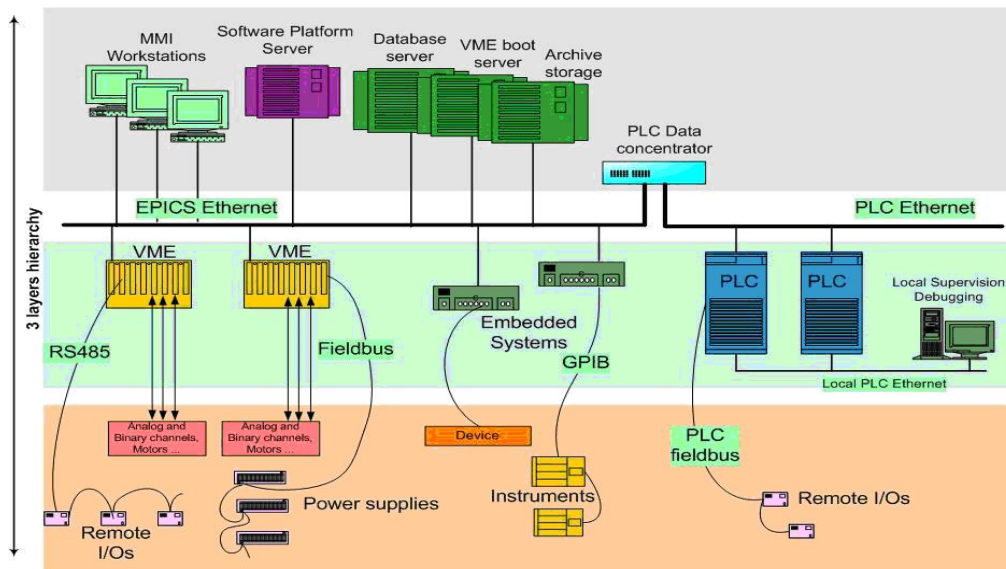


Figure 5.16: LIPAc standard local control system architecture

**Upper layer (Supervision).** At this layer, specific activities are performed (read a voltage, send a setting, start a diagnostic acquisition) either autonomously or under the supervision of the upper layer. This layer is mainly represented by the CCS and it is a common layer for all the LCSs.

**Intermediate layer (IOC).** At this layer, the systems will process the signals coming or sent to the accelerator devices. The IOCs can be either a VME system with a CPU connected to the network and various I/O boards for standard needs, or an embedded system (acquisition of diagnostics). For specific needs, embedded computers (diskless and fanless) running Linux with EPICS are used. Another alternative is to use PLC systems. This choice is very useful to manage functions related to the safe operation of the machine. The PLCs are connected to I/Os either with local I/O modules, OPC servers, or remotely with a proprietary Profibus fieldbus.

**Lower layer (Interfaces).** At this layer, the interfacing with the equipment will be done, either directly in case of fieldbus devices, or through an adaptation board (adaptation of signals, insulation ...). As it will be seen in the following sections describing the different LCSs, this general organization has been used to fit the particular needs of each subsystem

#### 5.4.6.2 LCSs common software tools

**Control System Studio (CSS),** based on Java language, is a framework which includes several tools to perform supervision compatible with EPICS. CSS is a modular framework that allows users to execute different tasks into the same environment, such as managing a device connected to the EPICS network through proper control panels, monitoring the PV's trends and so on. In general, CSS provides a high level of customization and new plugins can be developed to increase its features.

**Graphical User Interfaces.** The CSS Best Output Yet (BOY) GUI editor allows users to create a control panel using a set of widget that can be combined through drag and drop actions. By default, CSS has a set of widget that implements all the principal elements needed to create a GUI. All these widgets have a property to link them to EPICS PVs allowing the panel to monitor and control any equipment managed by EPICS.

The data browser implemented within CSS environment [111], interfaces nicely with other CSS tools. Users can seamlessly access samples from various data sources. Data browser displays the values of the variables over time.

**Backup and restore tool (BURT).** The ability of storing and retrieving setups of various parameters (used typically to store set-ups of the accelerator) is fulfilled by the Back Up and Restore tool (BURT).

**Archiver.** The CCS will provide a central archiver system. Before this final stage, every LCS can use a private archiver for commissioning needs. The archived data are stored (values, timestamps) on the Linux side either in files with a proprietary format or in a standard DB format.

**Nagios** is a powerful monitoring system that enables organizations to identify and solve infrastructure problems before they affect critical control system process. In addition to the regular surveillance on servers: CPU load, Ram, disk usage, a plug-in is available to monitor the EPICS PVs.

#### 5.4.6.3 LCSs integration

The integration policy is based in what each sub-system will provide its own local control system. These systems will be connected together on the same LAN. The Channel Access protocol will be used every time and everywhere between any elements of the control system, (IOC to IOC, Workstation to IOC, server to IOC), Fig. 5.17.

**LCS to CCS interfacing.** All subsystems will be seen with the native EPICS client software included in CCS (CSS for GUIs, Burt for backup/restore of parameters, channelArchiver for permanent parameters archiving, ...).

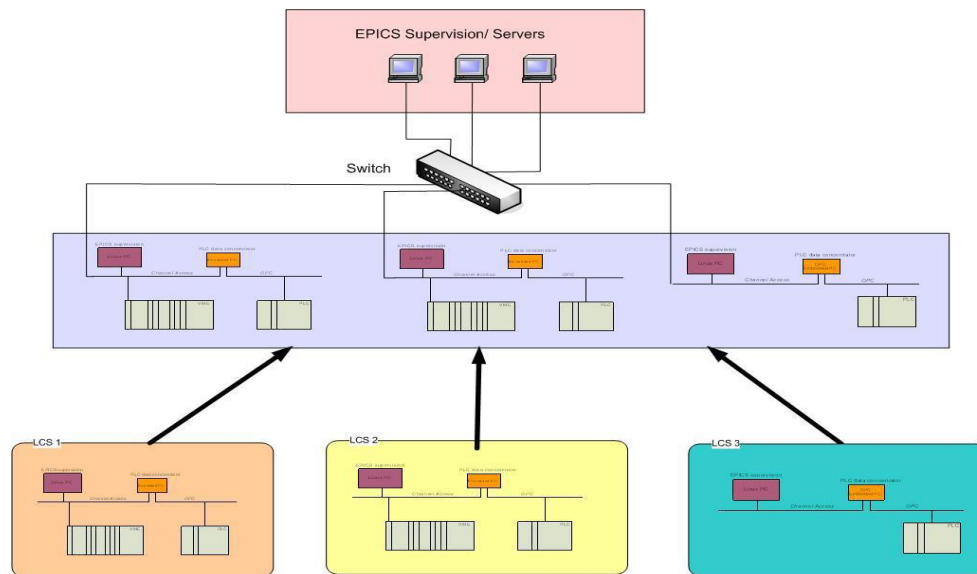


Figure 5.17: Subsystems integration

**LCSs to TS interfacing.** The interfacing will be done by coaxial cables giving triggers or gates to modules needing these timing signals (source, RF systems, diagnostics).

**LCSs to LAN interfacing.** Each LCS will come with a free Ethernet connection on its private Ethernet switch. A cable will connect this point to the main installation switch. To ease commissioning for the LCSs developed, it is expected that a gateway open to the Internet will be available. Nowadays, safe technologies are available to permit a safe connection for authorized persons and reject all the other connection attempts.

**LCSs PLCs to Channel Access and CCS.** Since PLCs are present in most of the local control system, it was decided to use a common solution for the PLC-EPICS interfacing. The communication between the PLCs and EPICS is done by a combination of commercially available OPC server and server packages with a special EPICS device support (EPICS softI/O running under Windows Xp Embedded Version OS). Fig. 5.18 shows the software architecture inside the OPC embedded PC. This equipment is configured with two Ethernet port, one for PLC side communications and one for EPICS side communications. Several PLCs can be managed by a single OPC server [10].

PLCs in charge of critical functions are connected to remote I/Os subsystems with a fieldbus. They have a local supervision system for debugging purpose. An OPC server will be the connection point between the PC Ethernet network and the PLC Ethernet network enabling to feed EPICS databases with data coming from the PLCs.

The OPC embedded PC will also be a gateway between the Ethernet network for the PLCs and the Ethernet network for EPICS. The EPICS database reflecting the PLC variables is generated by using two particular files:

- a CSV file having all the EPICS Process Variable configurations needed to create the final EPICS database file.

- a XML file having all the PLC parameters loaded in the PLC sub-systems, including hardware signals managed by the PLC.

The database is automatically loaded when the embedded PC is booted, then making available to EPICS clients all the parameters of the PLC.

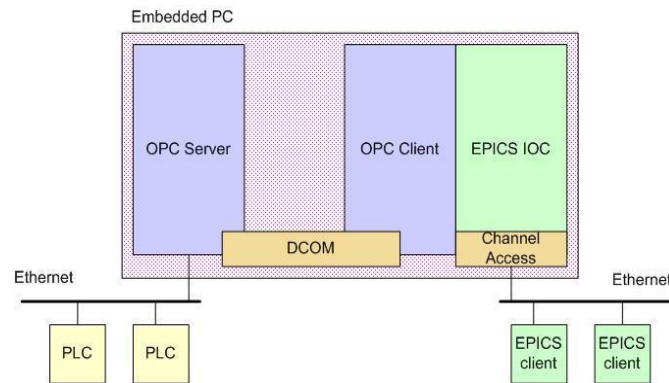


Figure 5.18: LIPAc OPC architecture [10]

## 5.5 Injector LCS

### 5.5.1 Injector (ion source and Low Energy Beam Transport (LEBT)) subsystem description

A 140 mA deuteron beam will be produced and extracted from an Electron Cyclotron Resonance (ECR) ion source, installed on a High Voltage (HV) platform. A Low Energy Beam Transport (LEBT) section will guide and match the deuteron beam from the ion source to a Radio Frequency Quadrupole (RFQ) accelerator, see injector overview in Fig. 5.19.

The injector aims to demonstrate that the performances expected for the final IFMIF injector are reachable. It has to deliver sufficient current to the RFQ to achieve a 125 mA RFQ output current. Due to expected beam losses in the RFQ, this current value requires that the ion source produces 140 mA maximum deuteron beam with excellent beam quality (transverse emittance). Injector requirements and target values are shown in Table 5.1.

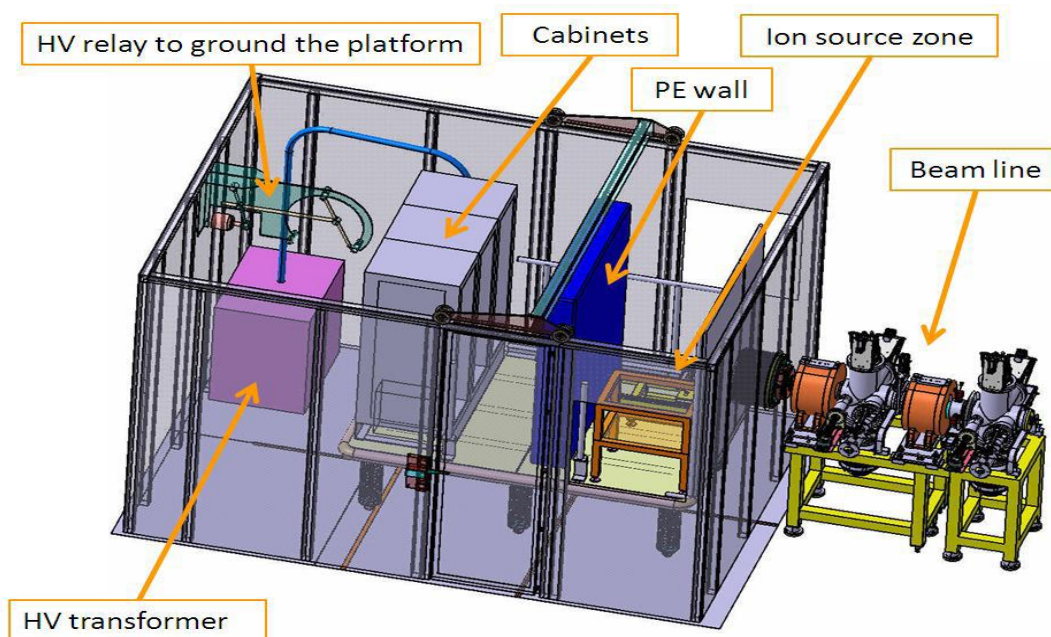


Figure 5.19: Overview of the ECR source installed in the high voltage (HV) cage and the LEBT line

#### 5.5.1.1 Functional scheme and description

The ECR conditions are created in the plasma chamber (part of the source mechanics (5), see Fig. 5.20). Depending on the ions required, deuterons (Deuterium) or protons (Hydrogen) production, the corresponding gas is injected (7) in this chamber. The RF is produced by a magnetron (2.45GHz, 1200Watts) and transported to the chamber by RF guides (2), see Fig. 5.20. In the chamber the magnetic field is created by means of two coils (6) fed by two 125A power supplies located around the plasma chamber in order to generate a magnetic field which, combined with the RF wave, produces the resonance for the plasma establishment.

Table 5.1: Requirements and target values for the injector

Requirement	Target value	Comment
Particle type	$D^+$	$H_2^+$ production will be experimentally determined
Output energy	100 keV	Fixed by the RFQ acceptance
Energy stability		
Output D+ current	140 mA	Assumes an RFQ transmission $\geq 90\%$
Operating current range		
Species fraction $D^+$	99%	At the output of the LEBT
Beam current noise	1% rms	At frequencies below $\approx 1\text{MHz}$
Normalized rms transverse emittance	$0.25\pi\text{ mm mrad}$	At the output of the LEBT
Duty factor	100%	Possibility of pulsed operation
Beam turn-off time	$\leq 10\mu\text{s}$	From 100% to 0% beam intensity

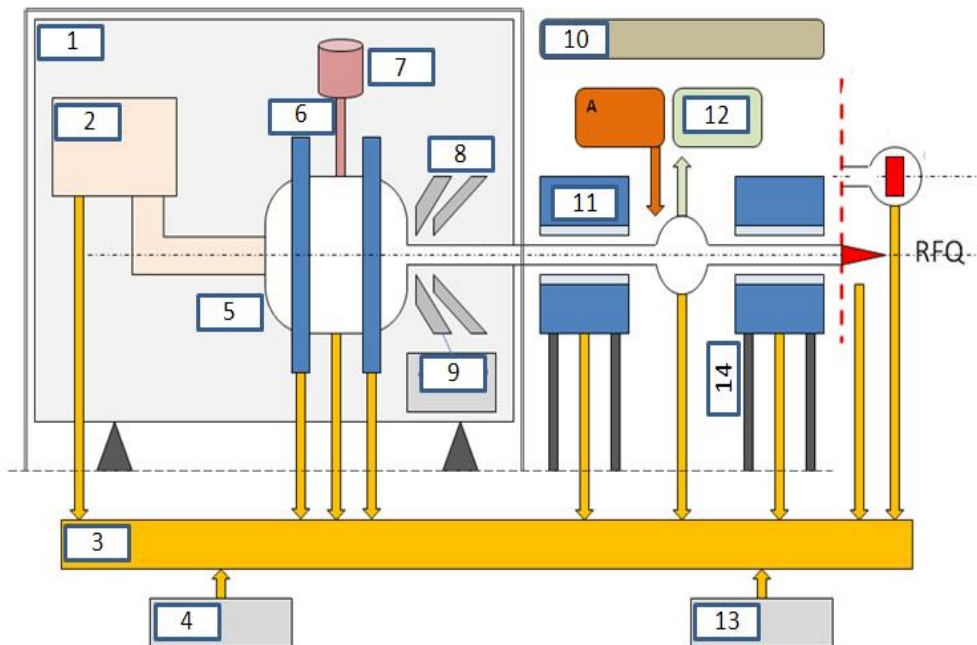


Figure 5.20: Functional scheme of the injector



The accelerator column (8) extract, accelerate and transport ions up to the LEBT entrance. All the equipments electrically connected to the source side of the accelerator column are located on the HV platform (1) biased to 100 kV, an intermediate electrode at a potential up to 50kV is used to extract the beam. A HV cage prevents access to the HV elements.

The LEBT section (10, see Fig. 5.20) transports and properly focuses the beam up to the RFQ entrance by means of two solenoids (11). A heavy-gas injection is connected to the vacuum chamber (14) in order to control the space charge compensation of the beam. The transport is optimized for the *wanted* ions ( $D^+$  in normal conditions). Other ions extracted from the source are mostly lost along the line that must be cooled down. The cooling system of the injector (3) removes heat loads from the magnetron, the plasma chamber, the magnetic elements (source coils and LEBT solenoids), the LEBT vacuum chamber, the Faraday cup (during commissioning) and the power supplies.

A vacuum system (12) is connected to the LEBT chamber. A beam chopper is also installed between the two solenoids. It will provide an enough short and proper beam pulse during pulsed operation of the accelerator.

### 5.5.2 Injector LCS requirements and design

The injector requirements are given by three elements, the ECR source, the LEBT and the diagnostics required for the operation.

**ECR source.** The goal of the source, is to produce a continuous beam of deuterons (or protons for test purposes), up to 140 mA with an energy of 100 keV. To interface the different equipment of the source, several solutions are used due to the variety of devices and the interface/protocol they support:

- HV 120kV power supply: interfacing done in Modbus-TCP. A Cometh module transforms the Ethernet to RS232
- RF system : interfacing done in Modbus-TCP. A Cometh module transforms the Ethernet to RS232 on the platform
- Automatic tuning unit: interfacing done in Modbus-TCP. A Cometh module transforms the Ethernet to RS232 on the platform
- Coils power supplies: interfacing done in Modbus-TCP. This interface is available inside the power supplies regulation module (so-called IOCASTE interface)
- Intermediate electrode: interfacing done by a specific Modbus-TCP crate. Its goal is to interface the analog/binary signals available at the level of the power supply and provide them through the standard Modbus-TCP protocol. This crate is called MCPSC (Modbus Crate for Power Supplies Control). It is located on the HV platform
- Gas injection ( $D_2$  or  $H_2$ ): driven by a flow controller and a MKS-PR4000 controller. Two safety valves are used and connected to the PPS for  $D^+$  beams safety

Only one Ethernet optical fiber is going to the HV platform. The distribution to the different devices is done with an Ethernet switch

**LEBT.** Its goal is to extract the beam from the source, to focus and steer it for injection into the RFQ stage.

- The extraction system, located between the source and LEBT, is composed of an intermediate electrode (puller), a repeller electrode and a ground electrode.
- The LEBT focuses the beam with 2 solenoids, each of them having an horizontal and vertical beam steerers.
- A flow controller is used to inject krypton in the chamber.
- The LEBT vacuum is done with 2 pumping units.

To interface the different equipment of the LEBT with the control system, several solutions are developed due to the variety of devices and the interface/protocol they support:

- Repeller electrode: interfacing done in Modbus-TCP with an MCPSC
- Solenoid power supplies: interfacing done in Modbus-TCP. This interface is available inside the power supplies regulation module (so-called IOCASTE interface)
- Beam steerers: interfacing done in Modbus-TCP with the MCPSC
- Pumping units: managed by a S7-300 Siemens PLC
- Krypton flow controller: interfacing done in Modbus-TCP

**Diagnostics.** The goal of these devices is to make beam analysis and intensity measurement. These devices shall work in pulsed or continuous mode. The diagnostics are located in the LEBT and they are the following:

- Faraday Cup (FC)
- Space charge compensation measurement (FGA: Four Grids Analyzer)
- Alternative Current Transformer (ACCT) intensity measurement at the end of the LEBT
- In continuous mode, an additional diagnostic for beam measurement intensity is used. It is based on thermic properties of a water flow.
- Emittance measurement (Allison scanner type) used in pulsed and continuous mode. Several functions are to be fulfilled:
  - Linear ramp generator to deflect the beam.
  - A mechanical assembly which stepped across the beam
  - A dedicated FC to measure the beam at each step

- Optical diagnostic based on the light emitted due to the interaction of the beam with residual gas. Radiation hardened camera is used to avoid damage coming from the important neutron production in case of deuteron beam production.

Most of the diagnostics (except calorimetry) make use of the combination of the VME ICV108 controller board and of the ICV178 acquisition board. This combination allows acquisitions up to 1 Msamples/sec in 16 bits for 16 channels.

- FC : fast acquisition ICV108/ ICV178
- FGA : ICV150 + ICV108/ ICV178
- ACCT : ICV108/ ICV178
- Calorimeter measurement : temperature measurements done by a Kelatron K633 module for °C/Volts conversion
- Emittance-meter:
  - Deflection of the beam by 2 +/- 10kV TREK power supplies
  - Secondary electron repeller with a 200 V power supply
  - Motor driven by a MaxV VME board from Oregon Microsystems. Encoder reading with the same board
  - Beam intensity measurement with a fast acquisition system (ICV108 / ICV178 boards)
- Optical diagnostic: camera interfaces with Labview. Stand-alone system with no connection to the EPICS supervision.

### 5.5.3 Injector LCS architecture

The injector LCS architecture can be seen in Fig 5.21. This architecture consists of three layers, the first one (below) is the equipment layer, source and LEBT components, which have been already explained. The second layer of the architecture, VME and PLC IOCs with the OPC server are explained below. The upper layer, the EPICS supervision one corresponds with the Central Control System (CCS), it has main human-machine interfaces. It is a Linux PC running Control System Studio (CSS) and other top level EPICS applications for supervision.

**VME modules.** A standard ADAS 16 slots VME crate is used with 2 MVME5500 CPUs. One CPU in slot 1 is the master of the configuration and manages the fast acquisition (ICV108/ ICV 178). The slave CPU manages all the equipment. The MODBUS-TCP connection is established on the 100Mb/sec secondary Ethernet port of the CPU. The network on this port is configured as a sub-network. Each 1Gb/sec main Ethernet ports of both CPUs are connected to the general network of the facility. One 16 channels DAC VME board ICV714 is used to drive the emittance-meter power supplies, one 32 channels ADC VME board ICV150 is used for the readback of these power supplies. An OMS MaxV VME

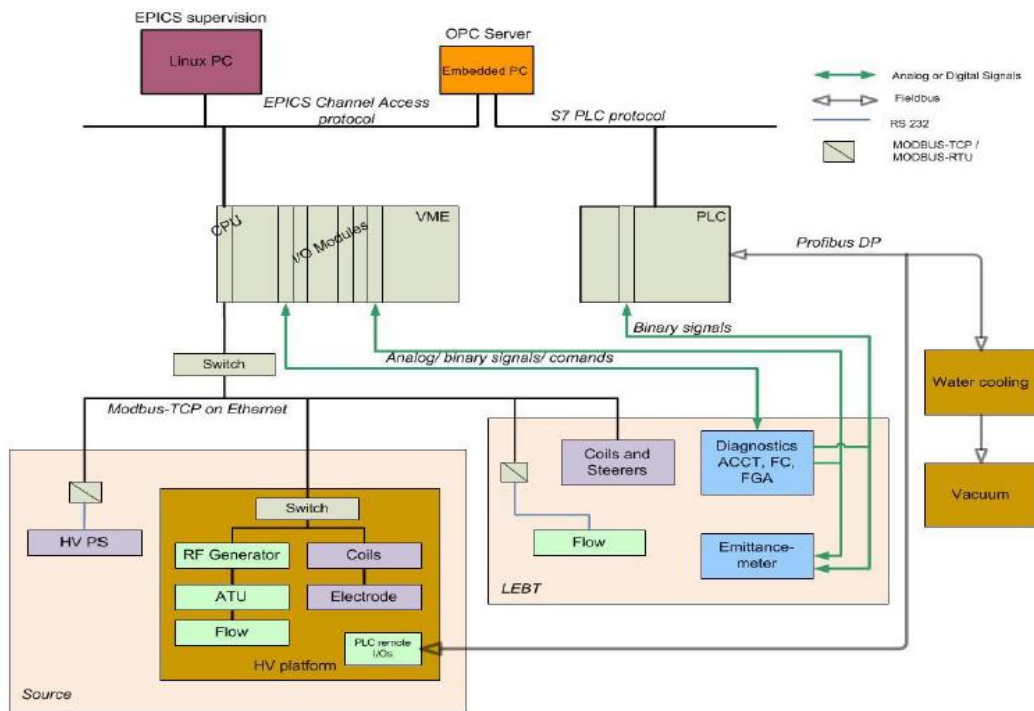


Figure 5.21: Architecture of the injector LCS

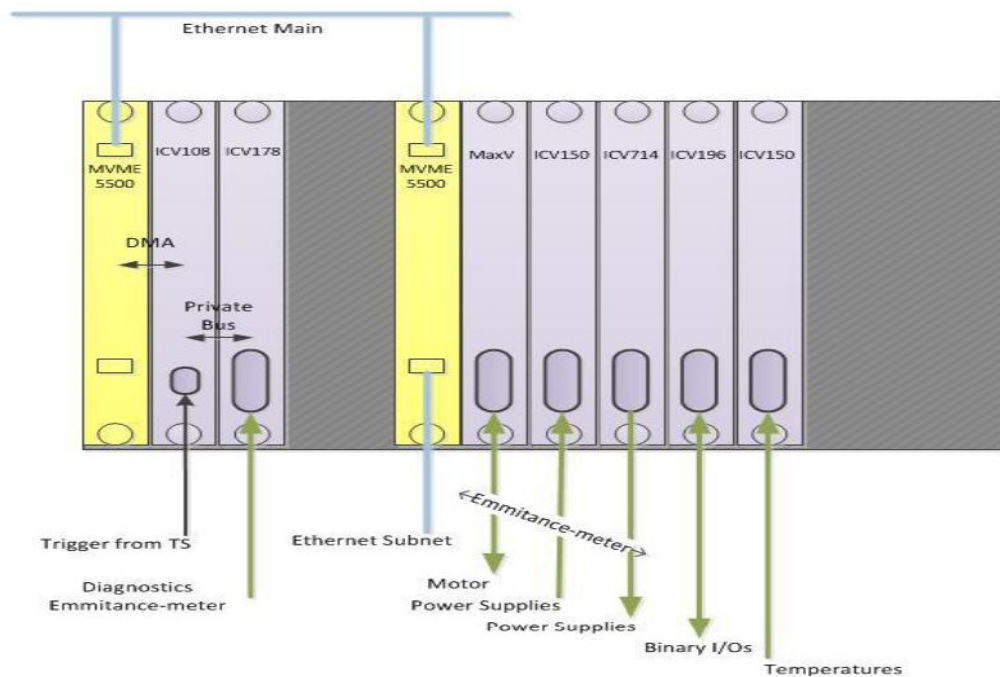


Figure 5.22: Injector VME configuration

board drives the emittance-meter motor. Finally, one of the 96 channels binary I/Os VME module ICV196 is used to send commands and receive status from various equipment.

The Modbus-TCP protocol is used for the control of power supplies and other devices over Ethernet. This protocol is very simple. It is a variant of the Modbus protocol, initially created for PLCs, which runs on serial lines.

The second port of the VME CPU is used for this purpose. It runs a sub-network with a private Ethernet addressing scheme. One Ethernet switch, on the ground level, distributes the network for the devices at ground level and for another switch at the HV level.

**PLC OPC Server configuration.** The PLC control system is based on a single CPU which is connected to local I/O modules installed in the same cabinet. It is also connected to the water cooling system, vacuum system and HV platform through Profibus DP connection. To avoid electrical insulation problem the connection between CPU and the HV platform remote module is made with optical fiber link. In addition to the elements explained before, PLC is also in charge of the water cooling and vacuum. These signals are transmitted by means of Profibus DP.

For the communication between the LEBT Siemens PLCs and EPICS, many solutions are available. The communication based on the OPC protocol is used, Fig. 5.18. This protocol uses Microsoft's COM and DCOM technologies to enable applications to exchange data using a client/server architecture. The OPC solution has the advantage to enable communications based on addressing symbol names rather than memory locations for the other ones.

The solution uses a Windows embedded PC running a combination of commercially available OPC server and server packages with a special EPICS device support. Thus, this alternative ensures a rapid and effective treatment of analog and digital signals that do not require complex operations. Furthermore, this solution allows to turn over the required signals to the EPICS Channel Access by a configuration that is highly reusable in other PLC based systems, more details of this integration are given in section 5.4.6.3.

**Timing system signals.** The timing signals sent to the source and diagnostics acquisition system are generated by the timing system.

- Source signal: used to drive the pulsed mode of the RF generator. It consists of a Transistor-Transistor Logic (TTL) pulse with a variable width from 1msec to 1sec.
- Trigger signal for pulsed acquisitions: used to trigger the acquisition of the fast acquisition system (ICV108/ICV178). It consists of a TTL raising edge, present even in continuous mode in order to provide always a starting point to the acquisitions.

## 5.6 Radio Frequency Quadrupole (RFQ) LCS

### 5.6.1 RFQ subsystem description

The RFQ subsystem is based on a  $\approx 10\text{m}$  Cu cavity able to transport, bunch and accelerate the continuous beam provided by the injector. This cavity has a dedicated support structure. The cavity along with its support structure, the vacuum system and cooling system (up to the heat exchanger) are the main parts of the RFQ. The slow tuning of the resonant frequency in the cavity is achieved by acting on the temperature difference between electrodes and external body of the cavity. The field level and field distribution in the cavity is monitored by pick up loops distributed along the cavity, RFQ overview is showed in Fig 5.23.

The goal of the RFQ subsystem is to validate the construction of a linear accelerator of RFQ kind, able to bunch and accelerate a deuteron beam current of 130 mA up to 5 MeV. Another challenge is to prepare a high quality beam to minimize beam losses in the following transport line and finally to simplify, as possible, the human intervention to service the RFQ itself. RFQ requirements and target values are given in Tab. 5.2.

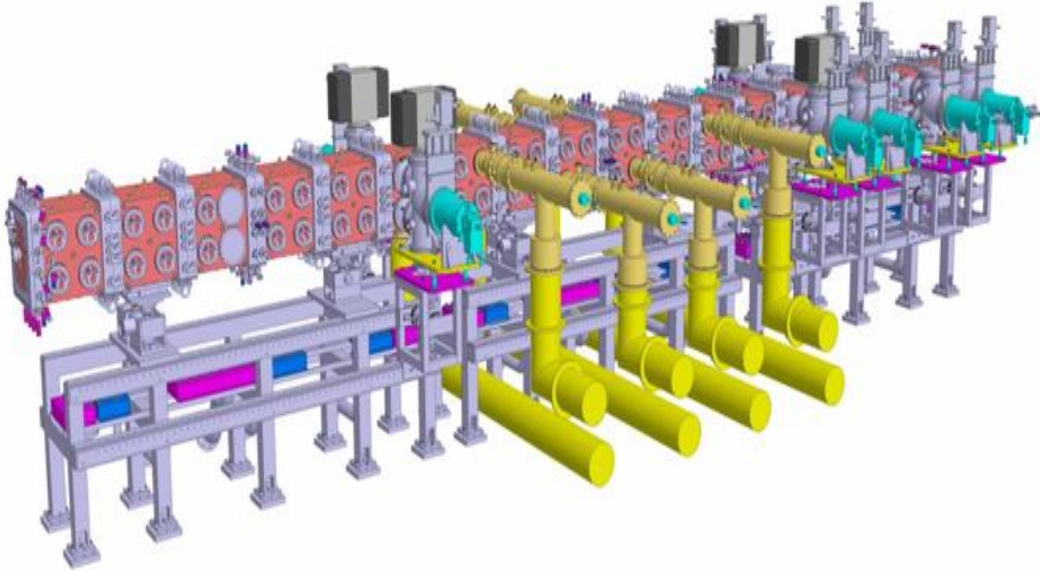


Figure 5.23: RFQ complete 3D model

Table 5.2: Requirements and target values for the RFQ

RFQ main parameters		
Requirement	Target value	Comment
Particle type	$D^+$	$H_2^+$ for testing (to avoid activation)
Input energy $\pm 100\text{keV}$	$\pm 100\text{keV}$	
Output energy $5\text{MeV}$	$\pm 50\text{keV}$	
Input $D^+$ current	$130\text{mA}$	
Output $D^+$ current	$125\text{mA}$	
Beam losses	$< 5\text{mA}$	$< 0.1\text{ mA}$ between $4\text{MeV}$ and $5\text{MeV}$
Input normalized emittance (r.m.s.)	$0.25\pi\text{ mm mrad}$	
Input Twiss parameters at RFQ input (cavity inner wall)	$A = 3\ B = 13.5\text{cm}$ $M < 10\%$	$130\text{mA } D^+$ current in total normalized emittance $1.5\pi\text{ mm mrad}$
RF Frequency	$175\text{MHz}$	In operation
Tuning range with water temperature	$\pm 100\text{kHz}$	Measured in high power tests on last modules
RF power dissipated in the RFQ copper	$100\text{keV}$	Fixed by the RFQ acceptance
Max heat transmitted at heat exchanger	$1000\text{kW}$	
Max surface field	$< 25.2\text{MV/m}$	1.8 Kilpatrick field (design criteria)
Output rms emittance (norm.) transv.	$< 0.30\pi\text{ mm mrad}$	At the RFQ output
Output rms emittance longitudinal	$< 0.2\text{MeVdeg}$	
Duty factor	CW	Pulsed operation for tune-up and start-up
Transverse zero current phase advance at RFQ end	$< 220\text{deg/m}$	(design criteria)
Longitudinal zero current phase advance at RFQ end	$< 90\text{deg/m}$	(design criteria)
RFQ Length	$9.814\text{m}$	
Maintainability	Hands on	
Vacuum tightness	$10^{-10}\text{mbar}$	For each module
Water circuits tightness@ operating pressure	$0.3\text{MPa}$	
RF field profile (quadrupole component)	$\pm 2\%$	Measured with bead pulling technique
Dipole /Quadrupole field component	$\pm 2\%$	
End of the RFQ main parameters table		

### 5.6.1.1 Functional scheme and description

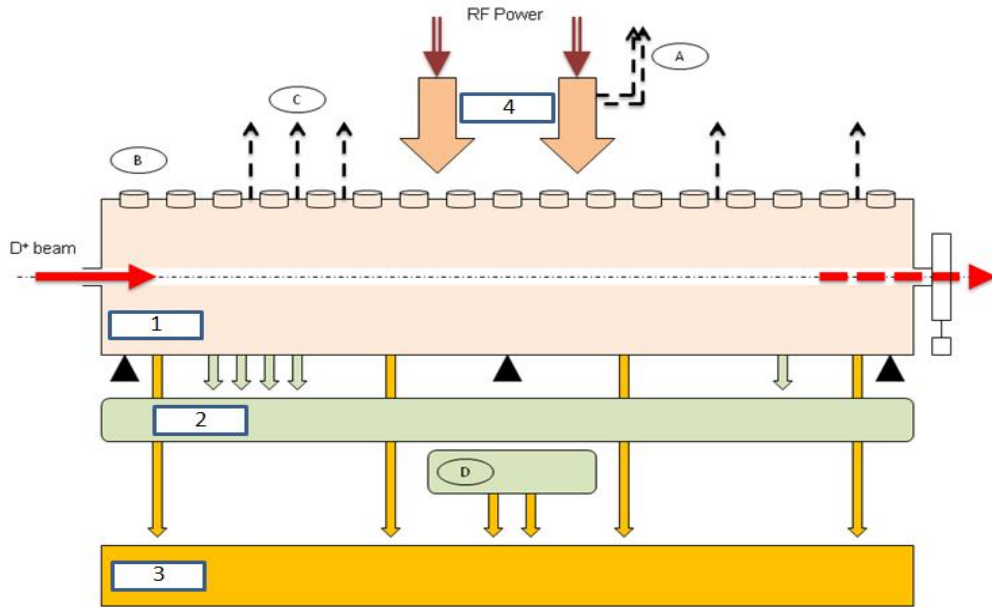


Figure 5.24: RFQ functional scheme

The RFQ operation is based on the RF fields created in the copper cavity (1, see Fig. 5.24), able to transport, bunch and accelerate the beam. This cavity has a dedicated support structure.

The RF power is injected into the cavity by means of RF Power Couplers [112] (4, see Fig. 5.24). Each RF coupler contains a set of RF diagnostics (A) connected to the RF chain LCS (arc detectors, bidirectional couplers and RF detectors to measure the forward and reflected power).

The RF tuning of this long cavity is performed by a complete set of tuners (B) that are machined after the module assembly. The field level and field distribution in the cavity is monitored by pick up loops (C) distributed along the cavity.

The heat generated by the RF and beam losses is extracted through a highly precise cooling system (2), which has also a role for the slow tuning of the resonant frequency in the cavity, by acting on the temperature difference between electrodes and external body of the cavity.

The vacuum conditions inside the RFQ, related to the gas load (mainly determined by beam losses), are sustained by vacuum system (3) based on cryogenics pumps. The cryogenics pumps compressors are water cooled (D, see Fig. 5.24).



### 5.6.2 RFQ LCS requirements and design

In order to achieve its goals, the RFQ has the following elements that must be specifically controlled by the LCS:

- **Cooling system.** The heat generated by the RF and beam losses is extracted through a highly precise cooling system which has also, as mentioned before, a relevant role for the slow tuning of the resonant frequency in the cavity. Then, cooling is composed by 7 water circuits (3 cold + 3 warm + 1 input lines) which allows to maintain stable the cavity RF frequency.
- **Surface temperature monitor.** Temperature information is used to monitor and verify eventual creation of hotspots related to current density peaks into the cavity. A uniform distributed sensor system is placed along the RFQ for mapping the surface temperature distribution, 240 temperature signals.
- **Vacuum system.** The vacuum conditions inside the RFQ, related to the gas load (mainly determined by beam losses), are sustained by vacuum system based on cryogenics pumps. The cryogenics pumps compressors are water cooled. Vacuum system is 6 pumping stations composed by 12 cryogenic pumps, 40 vacuum valves and 25 vacuum gauges, plus 3 removable pumping station (for a total of 295 analog and digital signals);
- **Slow and fast acquisition system for the RFQ cavity power.** For closed-loop control of the RFQ cooling system, dedicated signals coming from RF pickups are needed. The RF tuning of this long cavity is performed by a complete set of tuner. The field level and filed distribution in the cavity is monitored by pick up loops distributed along the cavity, there are RF signals coming from 44 pick-up and 16 directional coupler.
- **Bunch length monitoring system.** Since to bunch the beam is one of the main task of the RFQ subsystem, RFQ optimization consists in limiting as far as possible the losses in high energy, the maximum surface field and the power consumption. Therefore, to have information of the bunch length is essential. This monitoring system is based on electron collection from residual gas ionization by the beam and subsequent electron carriage on micro channel plate.
- **Send required signals to the LLRF control system.** More details on these signals are given in section [6.4.5](#).

To control the detailed equipment of the RFQ subsystem, several solutions are developed due to the variety of devices and the interfaces/protocols they support:

**Cooling, surface temperature and vacuum control.** Two different Siemens S7-300 PLCs perform the signals acquisition and control of vacuum plant and cooling system. Both PLCs are linked to an embedded PC running a Siemens OPC server for supervision needs.

RFQ water temperature can cause cavity deformation by modifying the resonation frequency. As consequence, a dedicated cooling control system composed by a PLC will control the temperature of 7 water circuits. Water temperature of each circuit can be modified with

a 3-port valve, in order to have better flexibility on the control algorithms. This PLC will be equipped with analog, digital I/O and PID boards.

**Fast acquisition control.** High-frequency parameters are acquired with proper hardware instrumentation based on high performance VME ADAS ICV108/178 boards.

**Bunch length monitoring control.** This monitoring system uses an embedded MicroIOC to control electrons energy analyzer and micro channel plates (4 input ADCs and 4 outputs DACs both 0-10V). This solution is cheaper and saves space compared to the equivalent VME system.

**LLRF control signals.** RFQ will provide several signals to LLRF, by means of EPICS Channel Access, in order to control the status and the tuning of the RFQ cavity. More details of the interface between RFQ and LLRF can be found in section [6.4.5](#).

### 5.6.3 LCS architecture

Following the explanations given before, the defined architecture can be seen in Fig 5.25. Equipment layer consists of the items described before which communicate with the intermediate layer using Profibus DP for the PLC, VME bus for the RF system and micro channels for the bunch length monitoring. In the middle layer all the IOCs are opened, one for the VME over VxWorks, one for MicroIOC which contains all necessary components to manage the device, such as RAM, Flash card, a power supply and a EPICS software control system installed and pre-configured, and finally one for the PLC over the embedded PC that implements OPC protocol and EPICS OPC client plus a startup file (st.cmd) to launch the IOC. This protocol uses Microsoft's COM and DCOM technologies to enable applications to exchange data using a client/server architecture. The OPC solution has the advantage to enable communications addressing symbol names rather than memory locations, more details of this integration are given in section 5.4.6.3. The upper layer, the EPICS supervision one corresponds with the Central Control System (CCS), it has main human-machine interfaces. It is a Linux PC running Control System Studio (CSS) and other top level EPICS applications for supervision.

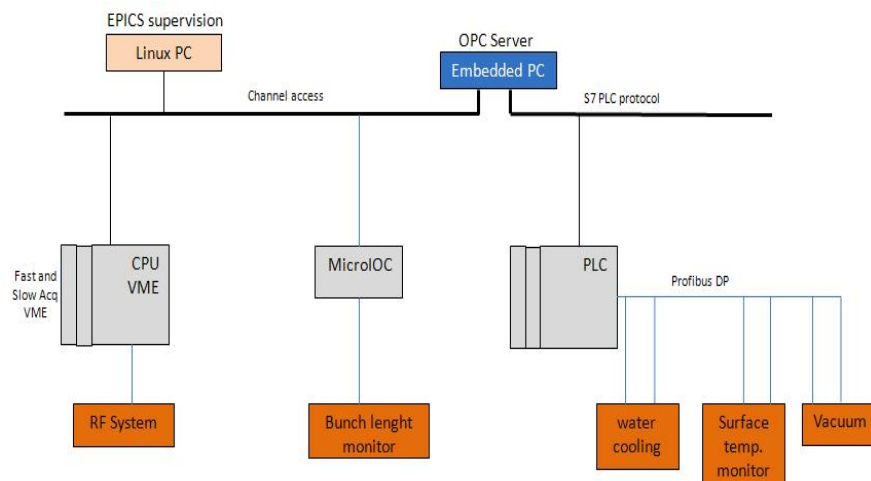


Figure 5.25: RFQ LCS architecture

## 5.7 Medium Energy Beam Transport (MEBT) LCS

### 5.7.1 MEBT subsystem description

The MEBT subsystem, Fig. 5.26, is responsible of the transport and matching of the RFQ beam into the SRF Linac. In order to minimize the beam losses caused by the strong space charge forces affecting the beam in this area, while keeping the sufficient freedom in beam optics optimization, a very compact scheme based in two sets of quadrupole magnets with steerers and two re-buncher cavities has been proposed [113]. MEBT main parameters are given in 5.3.

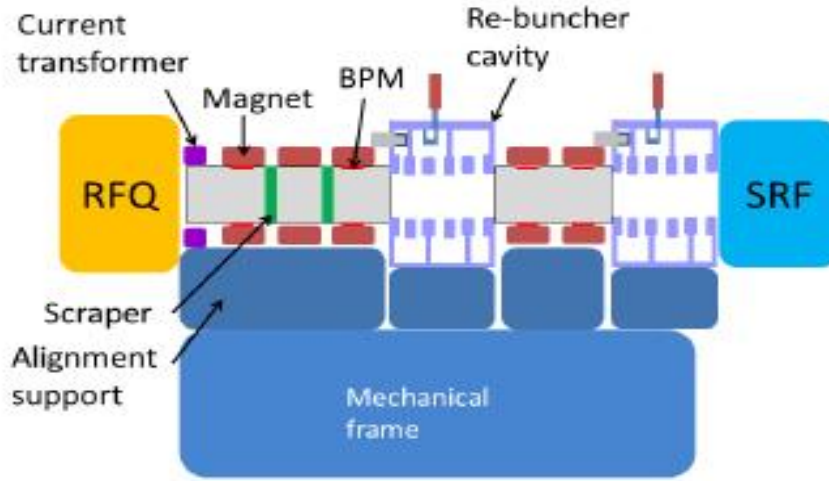


Figure 5.26: Schematics of the main components of the MEBT

Table 5.3: Requirements and target values for the MEBT

Requirement	Target value
Operating frequency	175 MHz
Beam A/q	2
Input energy/Output energy	2.5/2.5 MeV/u
Particle type	$D^+$ , $H^+$
Nominal beam peak current	125 mA
Beam dynamics length	235 cm
Buncher cavity voltage ( $E_0 LT$ )	350 kV
Coupler maximum transmitted power	15 kW
Quadrupole magnetic field gradient	25 T/m
Steerers strength (horizontal and vertical)	25 G.m

### 5.7.1.1 Functional scheme and description

The first function of the MEBT is to match the beam through the beam chambers (10), see Fig. 5.27, transverse and longitudinal. The longitudinal forces are applied to the beam by mean of 2 RF cavities (4). The RF power is injected into each cavity through a RF Coupler (9). Basically the frequency is adjusted in each cavity by an independent RF tuner (3), see Fig. 5.27.

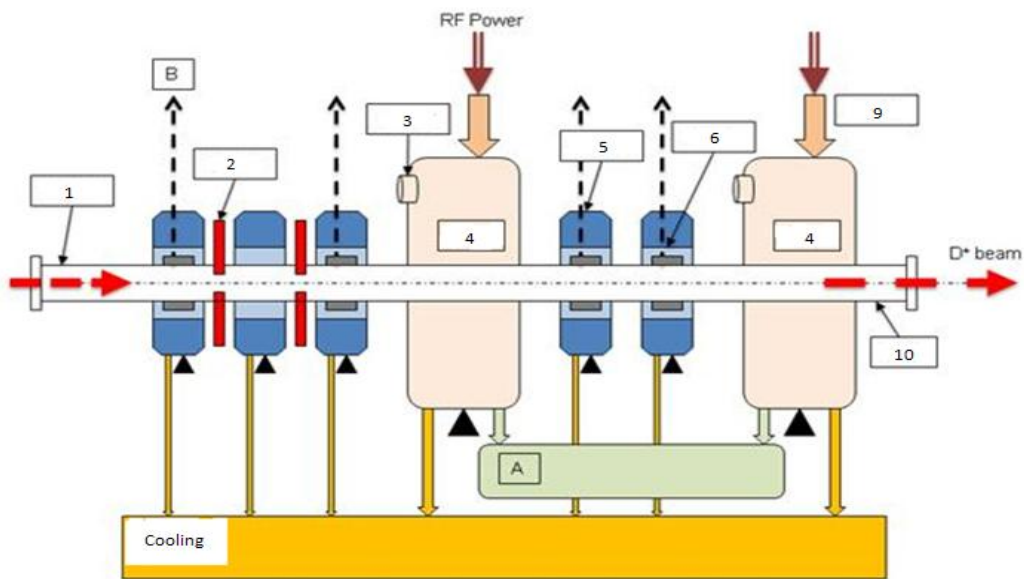


Figure 5.27: Functional scheme of the MEBT

The radial dimensions of the beam for injection into the SRF Linac are shaped by 1 quadrupole triplet and 1 quadrupole doublet (5). The transverse position of the beam is corrected by the magnetic steerers (6), see Fig. 5.27, located inside the quadrupole.

The beam center is measured by a Beam Position Monitor (BPM) (B) according to the balance of the beam magnetic field.

In order to clean the beam and to locate beam losses, most of the unmatched particles coming from the RFQ will be collected by metallic plates, called scrapers (2).

Due to the energy deposition, a water cooling system (cooling) is required to remove the heat of the following MEBT parts: buncher cavities, quadrupoles and scrapers.

To achieve the vacuum conditions (vacuum chamber, 1) required by the proximity of the RFQ and SRF Linac, an adequate vacuum system (A) is installed.

### 5.7.2 MEBT LCS requirements and design

MEBT LCS development has been mainly made in the framework of the thesis, both the LCS architecture design and the EPICS control applications, besides the MPS configuration. The items to be controlled by the LCS are the following:

- **Bunchers:** There are two re-buncher resonant cavities, with power couplers to supply the RF to the resonator and a tuning system. That means temperature measurements for the water cooling and motion controls for the tuners (2 stepper motors) including position readbacks (linear potentiometers) and limit switches. The stepper motor would shift a copper plunger in order to keep resonance frequency constant during operation, potentiometers and limit switches are necessary to manage the motor. Cooling channels at the bunchers are used to keep copper temperature at 20 °C.
- **Scrapers:** Scrapers must stop the out-of-emittance beam particles before injection into the SRF Linac. Thus, they are movable items so they need motion control (8 stepper motors) including position readbacks (linear potentiometers) and limit switches. Scrapers are used to stop losses coming from the RFQ and clean up the beam before it enters into the SRF, thus, scrapers are movable devices used for this purpose, therefore, they need also stepper motors.
- **Quadrupoles:** Transverse and longitudinal focusing for the beam using quadrupoles and steerers. Therefore, the LCS must control settings and monitoring of the 5 quadrupole power supplies and the 8 steerers bipolar power supplies and temperature measurements for the water cooling. The beam size in the RFQ is small (phase advance 90 deg/m) while in the HWR-Linac the phase advance is comparatively lower (20 deg/m) where the distance is much longer between focusing sections. Consequently, the MEBT must have a very compact structure to limit the beam emittance growth. Thus, 4 quadrupoles are used for transverse focusing and one more is needed to limit the beam size in the MEBT itself.
- **Vacuum:** Vacuum system is necessary in order to keep the vacuum along the beamline and to make possible the transition between an acceleration structure to another. Thus, 4 pumping units and 4 valves to control and 10 gauges to read are used.

To control and to interface the detailed MEBT equipment with the EPICS Channel Access, several solutions are developed due to the variety of devices and the interfaces/protocols they support:

**Bunchers and vacuum measurement and status signals.** Signals related to water cooling, pumping, valves and gauges are controlled using a programmable logic controller (PLC). The PLC chosen is a S7-300 model.

For the communication between the MEBT Siemens PLC and EPICS, many solutions are available. The communication based on the OPC protocol is used, Fig. 5.18. This protocol uses Microsoft's COM and DCOM technologies to enable applications to exchange data using a client/server architecture. The OPC solution has the advantage to enable communications based on addressing symbol names rather than memory locations for the other ones.

The solution uses a Windows embedded PC running a combination of commercially available OPC server and server packages with a special EPICS device support. Thus, this alternative ensures a rapid and effective treatment of analog and digital signals that do not require complex operations. Furthermore, this solution allows to turn over the required signals to the EPICS Channel Access by a configuration that is highly reusable in other PLC based systems, more details of this integration are given in section 5.4.6.3.

**Motion control in bunchers and scrapers.** As mentioned before, there are 10 stepper motors, 8 for scrapers and 2 for bunchers. In the buncher case, each stepper motor is controlled directly by the LLRF system, but its status and diagnostics will be controlled by PLC of the system, in the same way as the status signals explained before. More details on MEBT and LLRF communication can be found in section 6.4.5

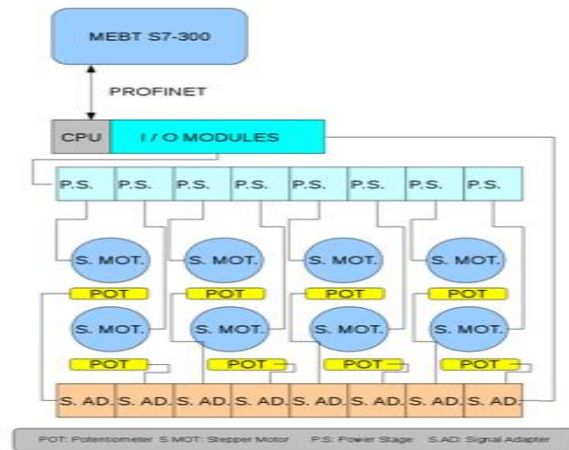


Figure 5.28: Scrapper motion control scheme in MEBT control system

The scrapers motion controls are managed by a Beckhoff system, see Fig. 5.28. A Beckhoff system is based on CPU CX1020 model with digital input/output modules for limit switches. The communication from the Beckhoff system to EPICS is carried out using the same PLC for the measurement and status signals, and from the PLC to EPICS, an OPC based solution.

The stepper motors should support certain levels of radiation, accordingly, not all the choices were possible solutions, McLennan and Phytron were discarded. Control choices based on Siemens FM353, cRIO and Delta-Tau were also studied but finally abandoned due to its compatibility issues with EPICS. Chosen solution allows to turn over the required motion signals to the EPICS Channel Access through and OPC protocol.

**Control of the power supplies in quadrupoles and steerers.** Regarding to power supplies, an interfacing with a serial protocol over Ethernet is the preferred solution. To interface power supplies with EPICS, StreamDevice is used. It is a generic EPICS device support for devices with a *byte stream* based communication interface. That means devices that can be controlled by sending and receiving strings (in the broadest sense, including non-printable characters and even null-bytes). Examples for this type of communication interface are serial line (RS-232, RS-485, ...), IEEE-488 (also known as GPIB or HP-IB), and TCP/IP. In order to achieve this control development, each power supply must have a 100BaseT Ethernet communication port (RJ45 connector) + TCP/IP and RS232 port (DB9 female connector) or USB 3.0 (USB standard connector) and a compatible communications protocol with Modbus/TCP. There are many choices for controlling power supplies but not many are able to fit with EPICS Channel Access. A serial control based on an EPICS generic device support such as StreamDevice is a quite standard and cheap solution. The only prerequisite

to achieve this solution is that these power supplies have a serial port communication and understand ASCII code. Power supplies were designed specifically for this project, therefore, its design fits with the needs of the control engineering.

In MEBT LCS, several signals are used to describe the status and the operation of devices and elements explained above through the adopted control solutions. Each one of these signals must correspond with an EPICS Process Variable (PV). A PV is a named piece of data associated with the machine (e.g. status, readback, setpoint, parameter) with a set of attributes. To achieve this equivalence, it is necessary to implement a device support which must be able to understand each device and to communicate with the EPICS Channel Access in order to write and read all process variables. In Table 5.6 several examples of this equivalence are shown. Fields in Table 5.6 have the following

- **Signal description:** Performance information of the signal.
- **Record type:** Type of record. Each record type has an associated set of record support routines depending on the record type. There are also some common properties to all records and some specific ones associated to some records types. These properties are referred to how monitors work, how scanning works, units data type, data precision, etc.
- **PV name:** Name of the process variable which runs through the Channel Access. This name must be unique to avoid collisions. It also must follow a naming convention to standardize the names circulating in the LIPAc Channel Access.
- **EPICS device support:** Type of software support used to develop the control of the device to which the signal described corresponds. Device support takes care of the hardware specific details of record support.

### 5.7.3 MEBT MPS

In the design of each LCS, there are several signals which should go to MPS system. These signals come from certain elements which are essential for the proper functioning of the machine and whose malfunction can have disastrous consequences in seconds. The space available for the reception of the MPS signal space is finite, so the signals can be summed up as far as possible using logic gates. Some signals in the MEBT LCS that will inhibit the operation of the system by means of BRTZ, FBI or SBI, see 5.4.5 for more details, can be seen in Fig. 5.29. Some alarm signals are expected to occur only during low duty cycle operation, they activate the BRTZ inhibition method. More critical signals like focalization and vacuum require a complete and fast beam stop, these signals activate the FBI inhibition and the closing valve system (GVOI) if they are related to a vacuum fault. A moderate temperature oscillation alarm goes to SBI inhibition, a complete beam stop but not as fast as FBI and without using the crowbar discharge.



Table 5.4: Examples of PVs for the MEBT LCS

Signal description	Record type	Process variable name	EPICS device support
Set current of power supply for Quadrupole	Analog output	MEBT:Q_PS1:SetCur	StreamDevice
Readback temperature of Quadrupole	Analog input	MEBT:Q_PS1:TRdbk	EPICS OPC Server/Client
Status of power supply for Quadrupole	Binary input	MEBT:Q_PS1:Stat	StreamDevice
Set current of power supply for vertical steerer	Analog output	MEBT:VSTR1_PS:SetCur	StreamDevice
Set current of power supply for horizontal steerer	Analog output	MEBT:HSTR1_PS:SetCur	StreamDevice
Overpressure on the gauge controller	Analog input	MEBT:VALVE1:OverP	EPICS OPC Server/Client
Open gate valve pump	Analog output	MEBT:VALVE1:CmdOpen	EPICS OPC Server/Client
Readback position of Stepping motor	Analog input	MEBT:SM1:PosRdbk	EPICS OPC Server/Client

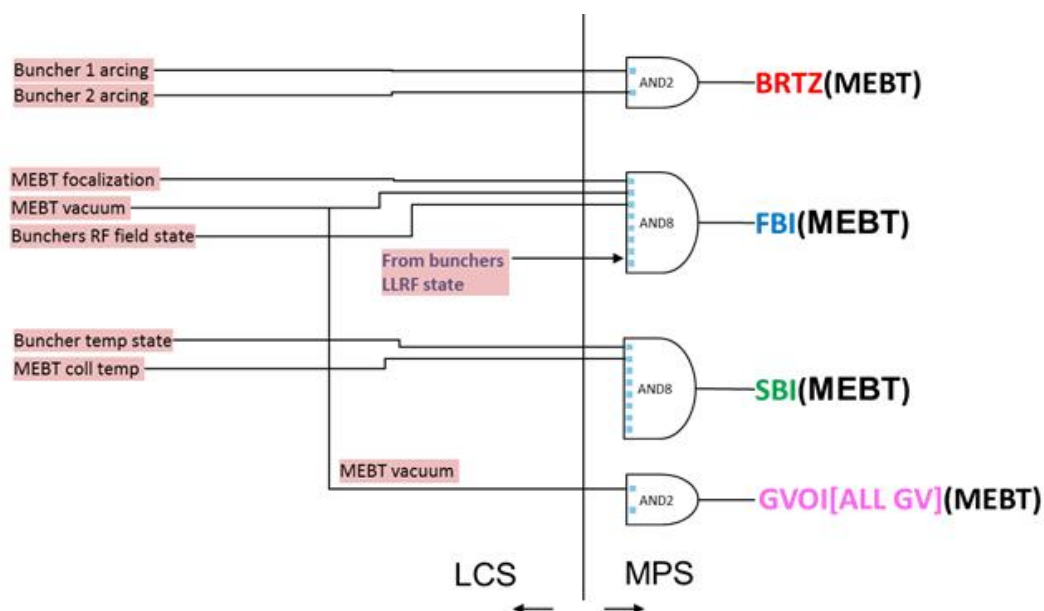


Figure 5.29: MEBT MPS logical diagram

### 5.7.4 MEBT LCS architecture

The final architecture can be seen in Fig 5.30. The equipment layer is composed by the magnets power supplies. It also has the motors drivers, potentiometers and limit switches for scrapers and bunchers, and finally the water cooling system for bunchers and scrapers and the vacuum system for bunchers.

With respect to the intermediate layer associated to the power supplies, an embedded Linux PC will launch the IOC. EPICS platform and StreamDevice support have been successfully tested on the embedded PC NEXCOM NISE 3500. This PC is Intel Core i7/i5 Fanless System with VGA, DVI-I, eSATA and one Expansion Slot. It is designed for a wide range of applications which demand intense work for extended periods of time with high reliability.

Stepper motors for the scrapers are controlled, as explained before, with a Beckhoff system which communicates with the PLC by means of Profinet bus. The intermediate layer which manages this Beckhoff system and opens the EPICS IOC is the mentioned OPC based configuration over an embedded Siemens PC. This IOC configuration is also used for the bunchers and scrapers water cooling and for the bunchers vacuum, because as can be seen, their signals are also controlled by the same PLC, using Profibus DP.

Stepper motors for bunchers are controlled by the LLRF system, more details of this configuration are given in section 6.4.5.

The upper layer, the EPICS supervision one, corresponds with the Central Control System (CCS), it has main human-machine interfaces. It is a Linux PC running Control System Studio (CSS) and other top level EPICS applications for supervision.

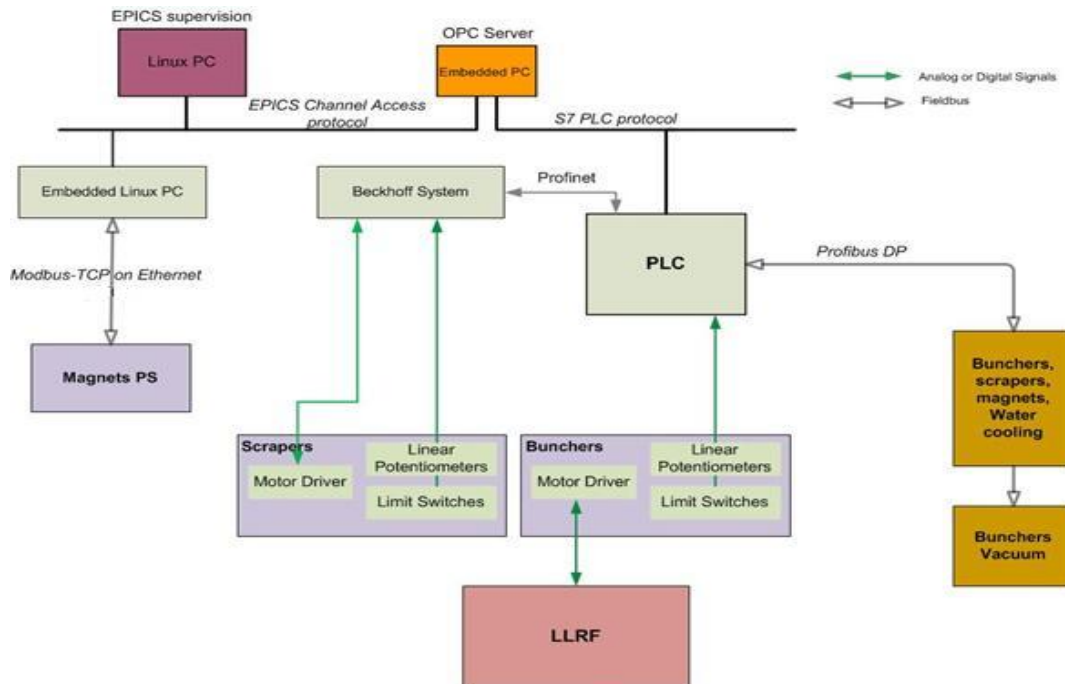


Figure 5.30: MEBT LCS architecture

## 5.8 Superconducting Radio Frequency (SRF) Linac LCS

### 5.8.1 SRF Linac subsystem description

The SRF Linac, see Fig 5.31, is a complex system around 6 m long, 2 m wide, and 2.8 m high, with a weight of about 15 tons. The SRF Linac is composed of 8 superconducting cavities (Half Waves Resonators, HWR) operating at 175 MHz to accelerate the deuterium beam from 5 to 9 MeV. Each cavity is powered with a 200 kW RF coupler working in continuous, and the beam is focused by 8 superconducting magnets. The frequency of HWR is adjusted precisely by using a mechanical tuner. The cryostat has the function of maintaining the temperature of the superconducting elements at 4.4 K, keeping the internal components under vacuum and insulating them from the external 300 K ambient temperature and atmospheric pressure, and shielding the HWR components from the earth magnetic field. This complete system also includes liquid helium supply, vacuum lines, supports, alignment systems, thermal shield, magnetic shield and instrumentation sensors. Table 5.5 shows a summary of the main functional specifications.

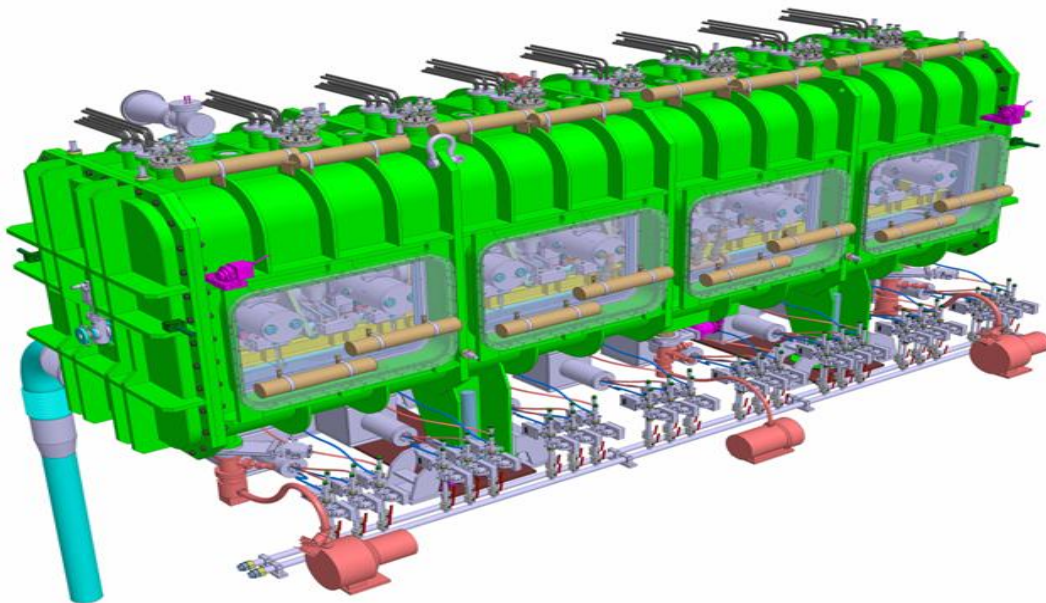


Figure 5.31: SRF Linac 3D model

Table 5.5: Requirements and target values for the SRF Linac

SRF Linac main parameters		
Requirement	Target value	Comment
<b>Beam at HEBT entrance</b>		
Operating frequency	175 Mhz	
Beam A/q	2	
Input energy/Output energy	5/9 MeV	
Input beam current	125mA	
Beam loss	< 10W	
Operating Temperature	4.4 K	
<b>Cavity</b>		
Accelerating field	5.0 MV/m	
Quality Factor	$1.4 \times 10^9$	at nominal field
<b>Solenoid</b>		
Magnetic field $B_z$ on axis	6.0 T	
Residual field at cav. flange	20 mT	
<b>Coupler</b>		
Transmitted Power	200 kW	TW mode: CW or pulsed (at every pulse widths) SW mode: pulsed only (pulse width: few tens of $\mu s$ , limited by circulator load)
<b>Cryomodule completed</b>		
Mechanical tolerance on beam axis positioning	$\pm 1$ mm	Alignment of the entire assembled structure, measured at 300K
Total tuner frequency range	100 kHz	
Accelerating field	4.5 MV/m	
HWR Quality Factor	$1.4 \times 10^9$	
Power transmitted by each coupler	200	These quantities are measured only on the coupler Test bench
External quality factor $Q_{ex}$	$< 6.3 \times 10^4$	(design criteria)
Magnetic field $B_z$ on axis	6.0 T	
He leak tests at RT	$10^{-12}$ hPa $m^3/s$	
Vacuum pressure at RT	$10^{-7}$ Pa	Gauge readout close to the pumping group
Vacuum pressure at 4.4 K	$10^{-8}$ hPa	Gauge readout close to the pumping group
<b>End SRF Linac main parameters table</b>		

### 5.8.1.1 Functional and scheme description

The SRF Linac transports and accelerates deuteron beam of nominal intensity from 5 MeV to 9 MeV in CW, by means of RF fields produced by 8 superconducting HWRs (1 in Fig. 5.32). The frequency of the HWR cavities is adjusted precisely by using an external mechanical tuner (A). The focusing and orbit corrections of the beam are made by 8 solenoids (9) and 8 steerers (8, Fig. 5.32). A solenoid together with steerers and a BPM (7) are gathered in a so called solenoid package (6).

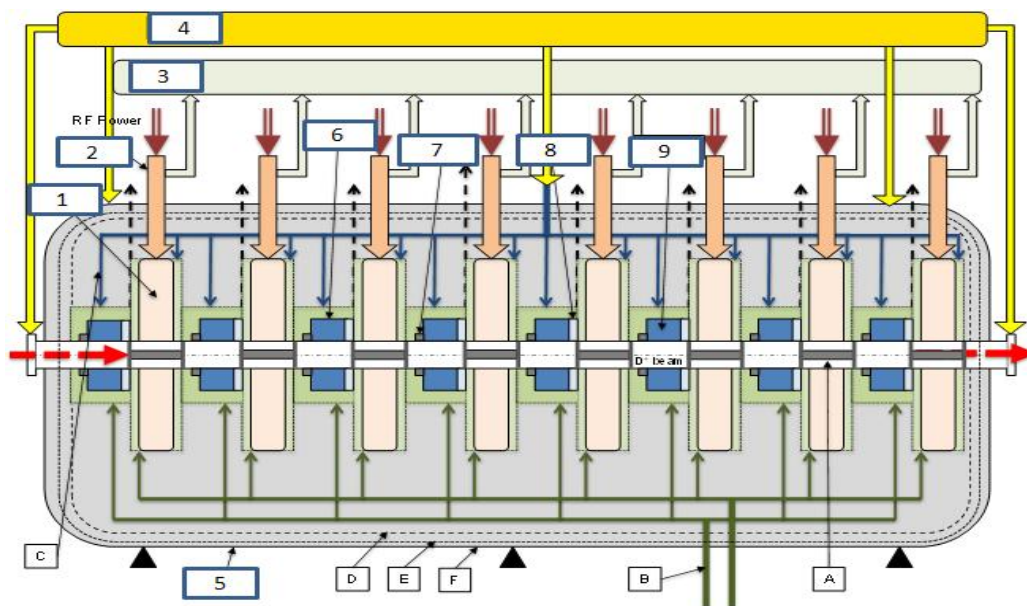


Figure 5.32: SRF Linac functional scheme

8 RF couplers (2) transfer the RF power into HWRs (coming from the RF power system). A water cooling system (3) removes the heat from coupler window area, antennas and tee-transition.

The cryostat (5, see Fig. 5.32) has the function of maintaining the temperature of the superconducting elements at 4.4 K, keep the internal components under vacuum and insulating them from the external 300 K ambient temperature and atmospheric pressure and shielding the HWR components from the earth magnetic field

The liquid helium circuit (B) injects cold liquid helium into 2 separate manifolds, one for the cavities and one for the coils. Internal piping dedicated to provide, LHe to the solenoid package current leads and GHe to the RF coupler outer conductor is not represented on this figure. A thermal screen (D) assure a transition at 60 K, by using helium gas, the magnetic shielding (E) protects HWRs from earth magnetic field and the overall vacuum tank (F) provides the required insulation. HWRs vacuum is assured by a dedicated vacuum system (C) sealed by 3 valves, and the insulating vacuum of the cryostat is sealed by 2 other valves, which are all using compressed air (4, Fig. 5.32).

### 5.8.2 SRF Linac LCS requirements and design

One of the main elements of SRF Linac LCS is the control of the solenoid package that has been mainly designed and developed in the framework of this thesis, both the LCS architecture design and the EPICS control applications, besides solenoid MPS configuration. As explained before, The LIPAC SRF Linac is a full-scale and operational cryomodule which contains all necessary equipments to transport and accelerate the required deuteron beam from an input energy of 5 MeV up to the output energy of 9 MeV. To ensure this functionality, many sensors and actuators are used, see sensors and actuators location in Fig 5.33. Thus, items to be controlled by the LCS are the following:

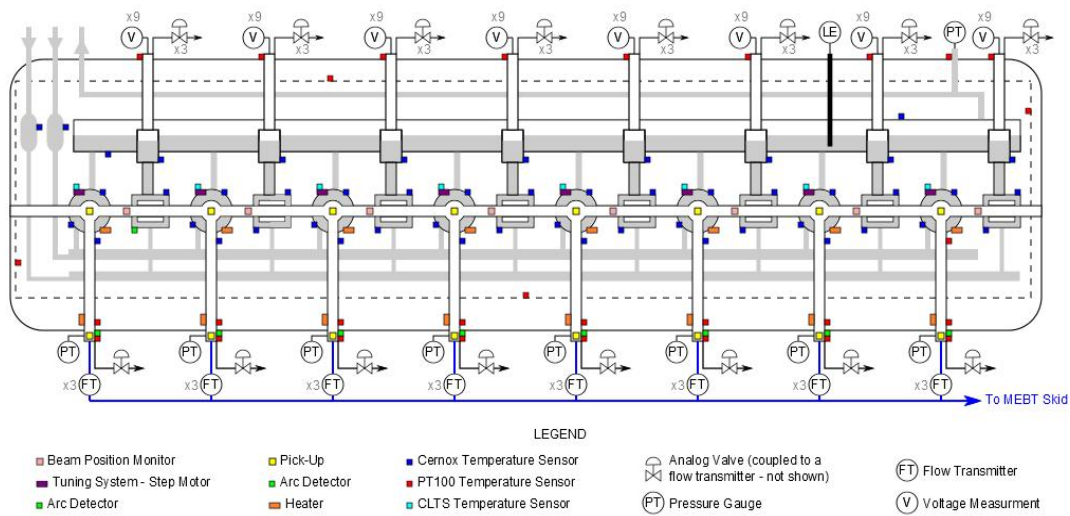


Figure 5.33: SRF Linac instrumentation

- Temperature sensors. The uniformity of temperature during cool down and operation can be an issue in this cryomodule. For this reason, it is mandatory to have many temperature sensors on all critical points and components of the system. To control temperature, PT100 technology is used to measure temperature over 40 K and Cernox technology to measure temperature below 40 K.
- RF pick-up on cavity. The RF pick-up is an antenna, with optimized length and positioning on the cavity, which measures RF level inside the cavity, without disturbing the field lines. Pick-ups are coupled to the LLRF system, which send orders to the stepper motors to adjust the cavity frequency. Each cavity is equipped with a pick-up. Each stepper motor is able to move a plunger in order to adjust the frequency of the cavity.
- Arc detector. One arc detector per RF couplers is foreseen, connected to the LLRF and used to rapidly switch off the RF power in case of arc discharges to avoid breakdowns.

- Vacuum gauges. The cryomodule vacuum insulation is done by 2 pumping groups. The beam vacuum is achieved by one pumping group. Electronics boards for vacuum monitoring are deported to avoid any damages due to the radiation level near the SRF Linac.
- Flow meters. Flow meters are used to monitor the helium flow of current leads, of RF couplers outer conductors, of phase separator, and also of the RF coupler antenna and window water flow.
- Analog valves. The analog valves are used to control the helium gas flow for current leads, RF coupler outer conductor, phase separator and also to control the fluids at the MCTL level. Valves will be located in the cryopant valve panel.
- Helium level. The liquid helium level needs to regulate the level of liquid inside the main phase separator tanks to the liquid inlet valves located in the main cryogenic transfer line. Only one sensor operates but 2 measurement channels will be installed.
- Pressure measurement. The pressure sensor which controls the pressure in the helium tank by regulating the gas outlet valve. The pressure sensor is installed on the safety circuit in the valve panel
- Heaters. A Heater on each cavity to simulate the RF power of the coupler when this one is off or below its nominal value in order to have a constant load on the cryogenic circuit. Another Heater on each RF couplers to regulate the temperature of helium gas flow at the outer conductor of RF couplers.
- Solenoid package. After each superconducting cavity, the focusing and orbit correction of the beam are performed by a set of solenoids and horizontal and vertical steerers. Each package includes a Cold Beam Position Monitor (CBPM), a solenoid and a pair of steerers (horizontal and vertical). In order to feed the solenoid and the steerers, 24 power supplies are used. CBPM for the SRF Linac will be installed inside each of the eight solenoid packages, between the half wave resonator cavities and the solenoids. They are in charge of the measurement of the position and phase of the beam centroid, its control will be described in the BI LCS, section 5.11. Another important element of the solenoid package are the current leads, they are used to drive the current to the magnets. Current leads are usually the dominant source of heat leaking into the magnet, therefore, the control of its temperature is crucial.

In short, each solenoid package is equipped with the following sensors or measurement devices:

- 2 Cernox sensors, one on the bottom of the helium tank of the solenoid, the other on the top of the tank, to control the temperature of the solenoid
- One Cernox sensor to detect liquid helium at the feet of the current leads
- An air venting system (fan) to avoid icing of the top flange of the current leads
- One PT100 on the top flange of the Solenoid Package to detect its eventual icing
- Three voltage measurements per set of coils (solenoid, horizontal steerer and vertical steerer)

The Cernox sensor measures the temperature of the feet of the current leads. In that case, the sensor is both used as a liquid detector and a temperature sensor. But its information is crucial as it will be possible to switch on the power supply of a solenoid package only if the current leads are cooled with liquid helium. The current will be reduced or stopped if voltage measurement between the two ends of one current lead is too high. A first threshold will trig an alarm and a second threshold will trig an interlock to switch off the power supply. The information about the current in the lead is also needed for mass flow regulation.

To control and to interface the detailed SRF Linac equipment with the EPICS Channel Access, several solutions are developed due to the variety of devices and the interfaces/protocols they support:

**Helium. Cold Box system control.** The Cold Box system is used to control the production of helium liquid. A Siemens S7-300 PLC controls and commands the dewar instrumentation, the compressor unit and the valves of the cryogenic transfer lines. All the connections with sensors and actuators are wired and based on analog and digital signals. The PLC Cold Box will be able to exchange data with the PLC Cryo via a Profibus DP network, see Fig 5.36.

**Cryogenic sensors, cooling. Cryo system control.** The Cryo system is used to control the cryogenic process. This system is used to manage all the sensors and actuators needed for the cooling down, nominal operation, warming up and abnormal situations where the fluid is directly the acting factor. All the liquid and gas loops used to cool down the solenoids and the cavities, to regulate the liquid helium level, to ensure the required gas mass flow for cooling of the RF couplers and for the current leads of the solenoid packages are part of the cryoplant. A Siemens S7-300 PLC controls and commands all the external and cryomodule sensors or actuators needed for the cooling down, nominal operation, warming up, and abnormal situations where the fluid is directly the acting factor. All the connections with sensors and actuators are wired and based on analog and digital signals. The PLC Cryo will be able to exchange data with the PLC Cold Box and PLC SRF via a Profibus DP network.

**Vacuum, pressure and temperature measurement. SRF system control.** The SRF system is used to control and monitor all actuators and sensors on cavities, couplers and vacuum. A Siemens S7-300 PLC controls and commands actuators and sensors concerning cavities, temperatures of the solenoids, vacuum, and pressure. The PLC SRF is linked to the OPC Server and also to the PLC Cryo via Profibus DP network. All the connections with sensors and actuators are wired and based on analog and digital signals. The PLC SRF will be able to exchange data with the PLC Cryo via a Profibus DP network.

**RF pick-up on cavities and stepper motors control.** The cavity frequency tuning system is activated with steppers motors, specifically chosen to be used inside extreme environment (under ultra-high vacuum and cryogenic temperature). Steppers motors will be controlled by a driver card with 2 externals signals. One signal will indicate the direction of the movement and the second one will be a train of pulses. Each pulse will indicate a step to be moved by the controller and then the motor. These 2 LVTTTL signals are sent by the LLRF, see section 6.4.5 for more details.

**Solenoid package control.** The current leads status control is achieved with a PLC. It has the same configuration showed above and it uses an OPC server to communicate with



the EPICS Channel Access using the above mentioned criteria.

Regarding to power supplies, an interfacing with a serial protocol over Ethernet is the chosen solution because, as mentioned before, this solution is a useful way to communicate this kind of devices with EPICS, besides, it is not an expensive solution since it only needs a PC to develop the control on it. To interface power supplies with EPICS, StreamDevice is used. It is a generic EPICS device support for devices with a *byte stream* based communication interface. That means devices that can be controlled by sending and receiving strings (in the broadest sense, including non-printable characters and even null-bytes). Examples for this type of communication interface are serial line (RS-232, RS-485, ...) and TCP/IP. In order to achieve this control development, each power supply must have a 100BaseT Ethernet communication port (RJ45 connector) + TCP/IP and RS232 port (DB9 female connector) or USB 3.0 (USB standard connector) and a compatible communications protocol with Modbus/TCP. There are many choices for controlling power supplies but not many are able to fit with EPICS Channel Access. A serial control based on an EPICS generic device support such as StreamDevice is a quite standard and compatible solution. The only prerequisite to achieve this solution is that these power supplies have a serial port communication. Power supplies were designed specifically for this subsystem, therefore, its design fits with the needs of the control engineering.

Several signals are used to describe the status and the operation of the solenoid package through the adopted control solutions. Each one of these signals must correspond with an EPICS Process Variable (PV). To achieve this equivalence, it is necessary to develop control applications which must able to understand each device and to communicate with the EPICS Channel Access in order to write and read all process variables. In Tab. 5.6 several examples are shown using the already mentioned criteria for the table fields:

Table 5.6: Examples of PVs for the SRF Linac LCS

Signal description	Record type	Process variable name	EPICS device support
Set current of power supply for solenoid	Analog output	SRF:SOL_PS1:SetCur	StreamDevice
Readback current of power supply solenoid	Analog input	SRF:SOL_PS1:CurRdbk	StreamDevice
Status of power supply for solenoid	Binary input	SRF:SOL_PS1:Stat	StreamDevice
Readback voltage for current leads	Analog input	SRF:SOL1_CL1:CurRdbk	EPICS OPC Server/Client
Readback temperature for current leads	Analog input	SRF:SOL1_CL1:TRdbk	EPICS OPC Server/Client
Readback voltage in vertical steerer	Analog input	SRF:SOL1_STR1:VRdbk	EPICS OPC Server/Client

### 5.8.3 SRF Linac MPS

In the design of each LCS, there are several signals which should go to MPS system. These signals come from certain elements which are essential for the proper functioning of the machine and whose malfunction can have disastrous consequences in milliseconds. The space available for the reception of the MPS signal space is finite, so the signals can be summed up as far as possible using logic gates. Some signals in the SRF Linac LCS that will inhibit the operation of the acceleration by means of BRTZ, FBI or SBI, see 5.4.5 for more details, can be seen in Fig. 5.34. Some alarm signals are expected to occur only during low duty cycle operation, they go to the BRTZ inhibition, i.e. arcs in the SRF cavity. More critical signals coming from a focalization fault and wrong level vacuum require a complete and fast beam stop, these signals activate the FBI inhibition and the closing valve system (GVOI) if they are also related with a vacuum fault. Another delicate issue to detect is the quench of the superconducting magnets. A quench is an abnormal termination of magnet operation that occurs when part of the superconducting coil enters the normal resistive state. This can occur because the field inside the magnet is too large, the rate of change of field is too large, or a combination of the two. Any quench alarm must completely stop the accelerator operation using the FBI inhibition method.

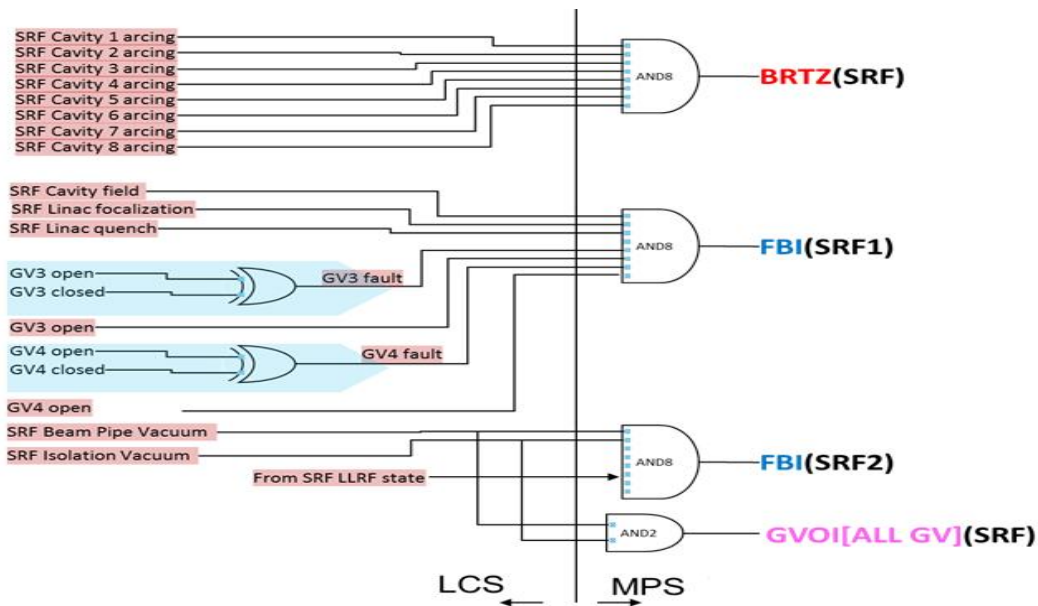


Figure 5.34: SRF Linac MPS logical diagram

### 5.8.4 LCS architecture

Solenoid control architecture can be observed in Fig 5.35. The equipment layer is mainly composed by the magnets and its power supplies and for the current leads and its temperature and voltage sensors.

In the intermediate layer associated to the power supplies, an embedded Linux PC will launch the IOC which support StreamDevice, the EPICS serial application for device support that has already been explained. EPICS platform and StreamDevice support have been successfully tested on the embedded PC NEXCOM NISE 3500. This PC is Intel Core i7/i5 Fanless System with VGA, DVI-I, eSATA and one Expansion Slot. It is designed for a wide range of applications which demand intense work for extended periods of time with high reliability.

A PLC is used to control the current leads and to communicate with other PLCs that manages the rest of the LCS. The IOC for the PLC is launched on an Siemens embedded PC which is connected with the supervision layer by means of the Channel Access, following the above mentioned criteria. The embedded PC has 2 Ethernet interfaces: one for the PLC connection, the second one for the EPICS/Channel Access connection. The upper layer represents the CCS with one Linux PC for supervision and EPICS support.

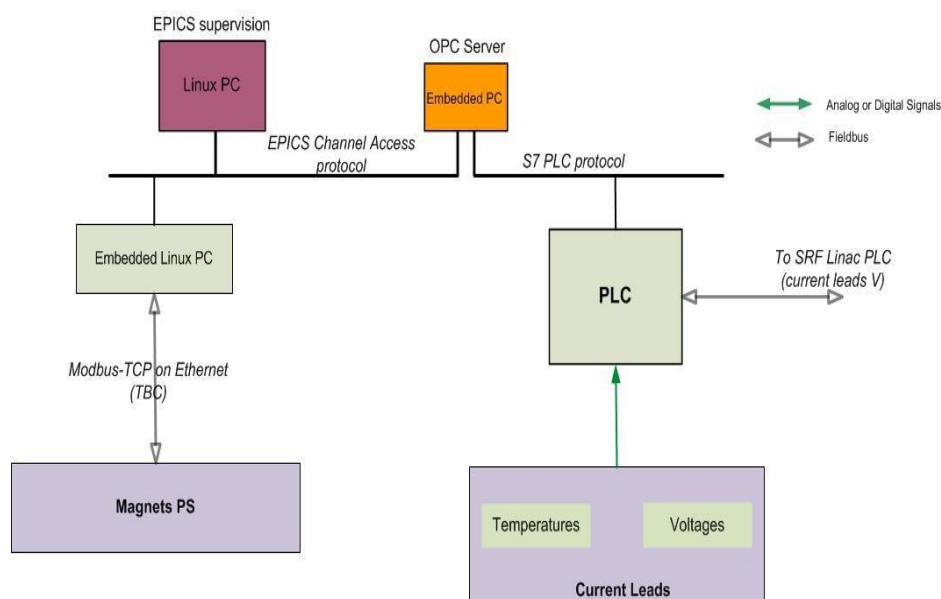


Figure 5.35: SRF Solenoid LCS Architecture

SRF Linac cryogenic distribution and vacuum system control architecture can be seen in Fig 5.36. It is a PLC based architecture which controls the different items explained before. The LHe distribution unit will use few independent PLCs for the cryogenic control process: one for the Cold Box (standard unit) and another for all the external and SRF Linac sensors or actuators needed for the cooling down, nominal operation, warming up, and abnormal situations where the fluid is directly the acting factor. The liquid and gas loops are under the responsibility of the LHe distribution unit to cool down the solenoids, to regulate the LHe

level and to ensure the required gas mass flow in the vapor cooled current leads and in the RF coupler heat exchangers.

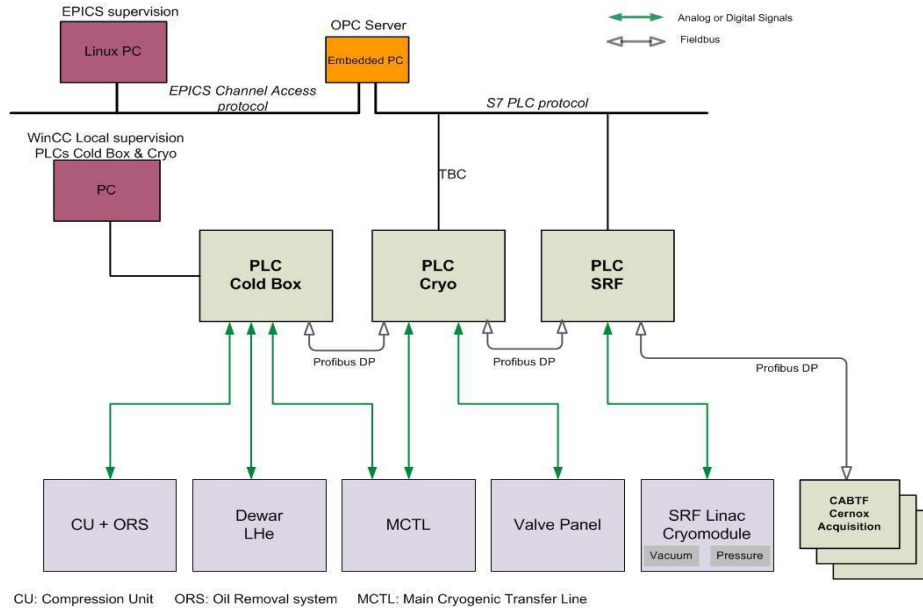


Figure 5.36: SRF Linac LCS architecture overview

Another PLC operates for the SRF Linac (vacuum, solenoids, correction coils, RF couplers and cavities) and shares some information with the PLC Cryo unit. The main part of the cryomodule sensors are supplied and read by specific PLC SRF Linacs. Their values (or any calculated references coming from the PLC RF System) can be numerically linked to the PLC Cryo via Profibus DP. For supervision needs, the PLCs is linked to an embedded PC running a Siemens OPC server and an EPICS OPC client. The embedded PC has 2 Ethernet interfaces: one for the PLC connection, the second one for the EPICS/Channel Access connection. A local supervision (WINCC) will be installed on the PLC Cold Box.

The upper layer, the EPICS supervision one, is common for both architectures and corresponds with the Central Control System (CCS), it has main human-machine interfaces. It is a Linux PC running Control System Studio (CSS) and other top level EPICS applications for supervision.

## 5.9 High Energy Beam Transport (HEBT) and Beam Dump (BD) LCS

### 5.9.1 HEBT and BD subsystem description

Last parts of the accelerator are the HEBT line and the BD. The aim of the HEBT line and BD is to manage the beam coming out from the SRF Linac and to stop it safely [114]. The HEBT line transports the beam from the SRF Linac exit to the BD, giving the required beam characteristics at the BD entrance. The HEBT line must also provide the space and beam conditions for the beam instrumentation needed to operate the accelerator and characterize the beam. The BD stops the beam (transforming its energy into thermal energy which is dissipated in a cooling system) and shields the resulting radiation [115]. See Fig. 5.37 and Fig. 5.38 for HEBT and BD respectively. Main requirements and target values are listed in Tab. 5.7

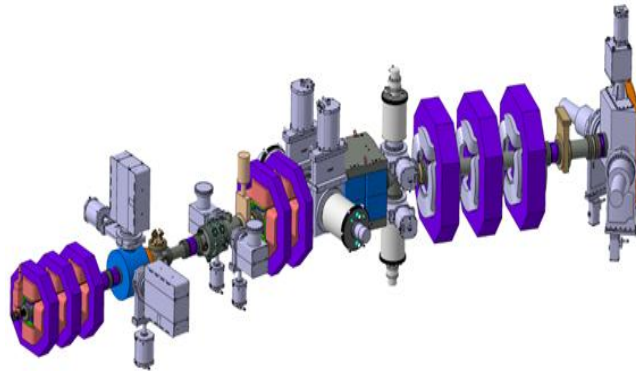


Figure 5.37: HEBT 3D view

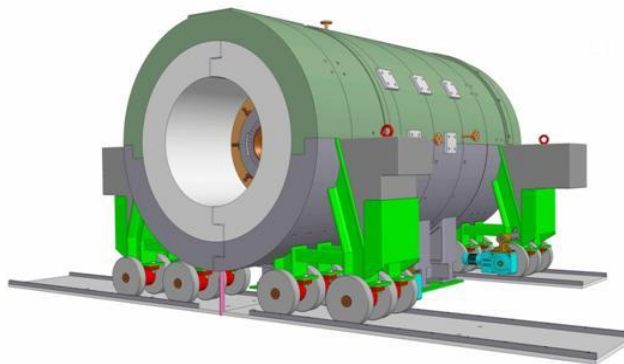


Figure 5.38: BD 3D view

Table 5.7: Requirements and target values for the HEBT and BD

HEBT and BD main parameters		
Requirement	Target value	Comment
Beam at HEBT entrance		
Species	$D^+$	$H^+, H_2^+$
Maximum beam current	125 mA	
Input beam energy	4.5 MeV/u	
Duty cycle	Up to 100%	
Beam properties at BD entrance		
Maximum beam axis displacement	10 mm	from nominal axis
Maximum power outside	1313 W	a radius of 15 cm
Maximum power density (CW)	70/320/300 W/cm <sup>2</sup>	at first 50 cm from BD aperture/Tip/ Rest of the cone
BD: Mechanical Tolerances		
Inner cone internal roughness	0.8 $\mu m$	
Inner cone circularity	0.4 mm	
Flow shroud circularity	0.4 mm	
Inner cone axis straightness	0.4 mm	
Flow shroud axis straightness	0.4 mm	
Thickness tolerance	0.4 mm	
Axis Alignment precision in assembly	0.4 mm	
Water circuit maximum pressure	$5 \times 10^5 Pa$	
Cartridge water maximum pressure	$4 \times 10^5 Pa$	
Maximum leak in cartridge vacuum test	$10^{-8} hPa.m^3/s$	(design criteria)
HEBT line		
QP Integrated Field on pole	0.108/0.0816/0.217 T.m	
Dipole magnetic field	0.31 T	
Steerers integrated magnetic field on axis	0.003 T.m	
End HEBT and BD main parameters table		

#### 5.9.1.1 HEBT and BD functional scheme and description

The beam going out of the SRF Linac is transported and characterized along the HEBT line up to the BD. The magnetic elements used are: quadrupoles (2, see Fig. 5.39) for radial focusing, steerers (4) for correcting beam radial position and a bending magnet (6) to deviate the beam. A set of diagnostics is distributed along the line.

At the end of the HEBT, a mechanical lead shutter (D) is installed in order to shield most

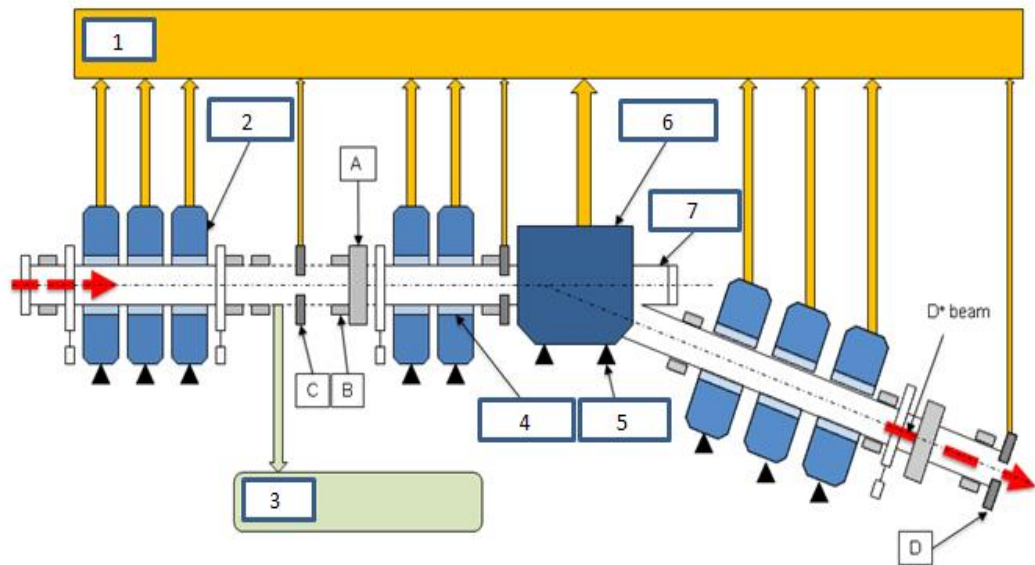


Figure 5.39: Functional scheme of the HEBT

of the gamma rays coming from the activated material [116] [117] of the BD cartridge during the maintenance periods. A scraper is also inserted to protect the beam tube inside the BD cell from abnormal beams that could damage it. A water-cooling system [118] is used to extract heat generated by ohmic losses in magnets (quadrupoles and bending magnet) and by beam losses in slits (C).

A vacuum system (3 see Fig. 5.39) is implemented to pump out chambers after installation or maintenance and to maintain acceptable pressure in accordance with adjacent sub-systems as well. On the scheme showed in Fig. 5.39, diagnostics are found in HEBT beam chambers (7), beam profilers (A), beam position monitors (B).

When stopping the beam (see Fig. 5.39), two aspects are essential: absorbing its continuous power and limiting the radiation emitted during and after operation. The beam particles are stopped in a copper layer (A, see Fig. 5.39) shaped as a cone to distribute the power and reduce the heat density. A fast water flow is running around the other side of this cone in order to transport the heat to the exchanger of the water-cooling skid (4).

The mechanical structure around the copper cone including the local water circuit is called the *cartridge* (3, see Fig. 5.39). Due to the water activation, a decay coil (5) is inserted between the cartridge and the skid. A multi material shielding (1) made of water, iron and polyethylene surrounds the cartridge in order to limit radiation generated by beam particle interaction with copper and induced activation.

The lower part of the shield acts as support of the whole assembly (2), Fig. 5.40.

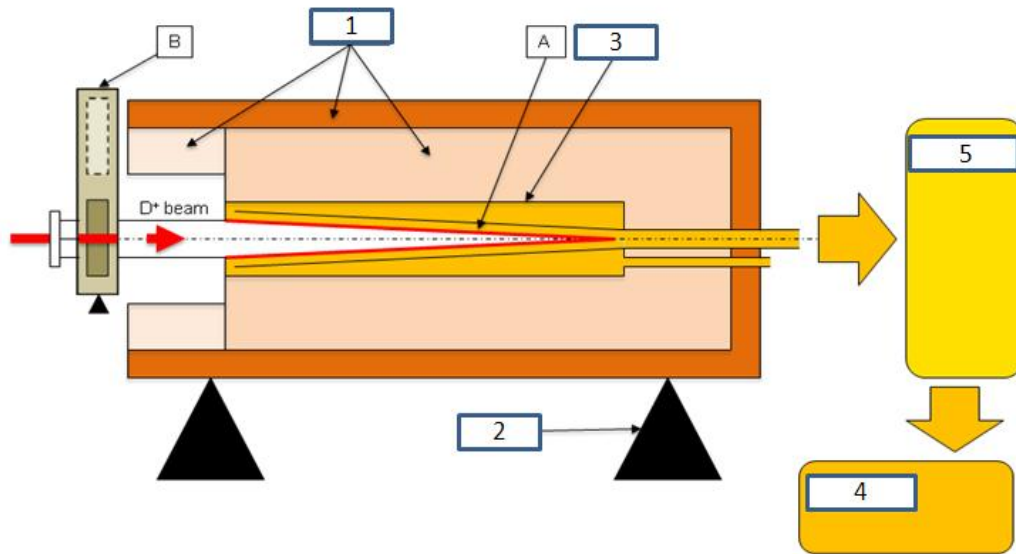


Figure 5.40: Functional scheme of the BD

### 5.9.2 HEBT and BD LCS requirements and design

HEBT LCS development has been mainly made in the framework of the thesis, both the LCS architecture design and the EPICS control applications, besides the MPS configuration. As explained, the main function of the HEBT is to characterize the beam and to transport it into the BD. The focusing is done successively by a triplet of quadrupoles, a doublet before the dipole and a triplet after the dipole. Therefore, concerning to the LCS, the following elements have to be taken into account in order to carry out the control:

- **Quadrupoles and dipoles:** A quadrupole triplet is inserted at the beginning of the transport line to handle the beam at the output of the SRF linac, correcting possible errors and adjusting the beam parameters before the diagnostic plate (D-plate). After the D-plate there is a quadrupole doublet used to focus the beam and to provide additional focusing during the quadrupole scan emittance measurements. Then, a bending magnet is inserted in the line mainly to avoid a direct line of sight for backscattering radiation. At the end of the HEBT there is a quadrupole triplet to expand the beam and to obtain a manageable power deposition density on the beam dump. There two pairs of horizontal/vertical dipole correctors (steerers) in each group to correct the beam trajectory. All these magnets are fed by power supplies which need to be controlled.
- **Lead shutter:** to shield the gamma radiation which comes from the activated beam dump trough the beam in the last drift before the beam dump cell. The shutter will need 2 binary outputs (command) and 2 binary inputs (status sent to MPS/PPS) from a external PLC.



- Vacuum system: pumps, isolation valves, fast valve for linac protection and instrumentation. Vacuum control.
- Scraper located before the BD: fixed position, monitoring of temperature (thermocouples). Fixed scraper, it is not a movable device, it do not require motion control.
- Cooling of magnets and BD. The flow will be dependent of the duty cycle. Two different cooling control system, one for the beam dump and one for the magnets of the HEBT.
- BD instrumentation (protection): 6 Hydrophones which will monitor the hot points of the BD (bubbles in the cooling water), 6 radiation chambers for characterization of the beam position and shape.

To control and to interface the detailed HEBT and BD equipment with the EPICS Channel Access, several solutions are developed due to the variety of devices and the interfaces/protocols they support:

**Power supplies control for magnets (quadrupoles and dipoles).** Regarding to power supplies, an interfacing with a serial protocol as over Ethernet is the preferred solution following the above mentioned criteria in a similar situation. Thus, to interface power supplies with EPICS, StreamDevice is used. It is a generic EPICS device support for devices with a *byte stream* based communication interface. That means devices that can be controlled by sending and receiving strings (in the broadest sense, including non-printable characters and even null-bytes). Examples for this type of communication interface are serial line (RS-232, RS-485, ...), IEEE-488 (also known as GPIB or HP-IB), and TCP/IP. In order to achieve this control development, each power supply must have a 100BaseT Ethernet communication port (RJ45 connector) + TCP/IP and RS232 port (DB9 female connector) or USB 3.0 (USB standard connector) and a compatible communications protocol with Modbus/TCP. Power supplies were designed specifically for this project, therefore, its design fits with the needs of the control engineering.

**Vacuum, cooling and BD protection system.** Signals related to water cooling, pumping, BD instrumentation, valves and gauges are controlled using a programmable logic controller (PLC). The PLC chosen is a S7-300 model. For the communication between the HEBT Siemens PLC and EPICS, many solutions are available. The communication based on the OPC protocol is used following the above mentioned criteria, Fig. 5.18. As mentioned before, this protocol uses Microsoft's COM and DCOM technologies to enable applications to exchange data using a client/server architecture. The OPC solution has the advantage to enable communications based on addressing symbol names rather than memory locations for the other ones. This solution uses a Windows embedded PC running a combination of commercially available OPC server and server packages with a special EPICS device support. Thus, this alternative ensures a rapid and effective treatment of analog and digital signals that do not require complex operations. Furthermore, this solution allows to turn over the required signals to the EPICS Channel Access by a configuration that is highly reusable in other PLC based systems.

In HEBT and BD LCS, several signals are used to describe the status and the operation of devices and elements explained above through the adopted control solutions. Each one of these signals must correspond with an EPICS PV. To achieve this equivalence, it is necessary

to develop EPICS control applications which must be able to understand each device and to communicate with the EPICS Channel Access in order to write and read all process variables, that is, all signals. In Tab. 5.8 several examples of this equivalence are shown.

- **Signal description:** Performance information of the signal.
- **Record type:** Type of record. Each record type has an associated set of record support routines depending on the record type. There are also some common properties to all records and some specific ones associated to some records types. These properties are referred to how monitors work, how scanning works, units data type, data precision, etc.
- **PV name:** Name of the process variable which runs through the Channel Access. This name must be unique to avoid collisions. It also must follow a naming convention to standardize the names circulating in the Channel Access.
- **EPICS device support:** Type of software support used to develop the control of the device to which the signal described corresponds. Device support takes care of the hardware specific details of record support.

Table 5.8: Examples of PVs for the HEBT and BD LCS

Signal description	Record type	Process variable name	EPICS device support
Thermocouples sensor in the inner cone of BD, temp. monitoring	Analog input	BD:CONE:T1Rbck	EPICS OPC Server/Client
Hydrophones in the cartridge. Pressure monitoring	Analog input	BD:CART:P1Rdbk	EPICS OPC Server/Client
Water flow. Pressure monitoring	Binary input	BD:P1Stat	EPICS OPC Server/Client
Water flow. Temperature monitoring	Binary input	BD:T1Stat	EPICS OPC Server/Client
Set the current for quadrupole 1	Analog output	HEBT:Q1_PS:SetCur	StreamDevice
Set the current for steerer 1	Analog output	HEBT:STR1_PS:SetCur	StreamDevice
Pump controller. Open gate valve pump	Analog output	HEBT:VALVE:CmdOpen	EPICS OPC Server/Client
Lead shutter position status	Analog input	HEBT:LEAD:PosRdbk	EPICS OPC Server/Client

### 5.9.3 HEBT and BD MPS

In the design of each LCS, there are several signals which should go to MPS system. These signals come from certain elements which are essential for the proper functioning of the machine and whose malfunction can have disastrous consequences in seconds. The space available for the reception of the MPS signal space is finite, so the signals can be summed up as far as possible using logic gates. Some signals of the HEBT and BD LCS that will cut off the accelerator operation by means of BRTZ, FBI or SBI inhibition methods (see 5.4.5 for more details) are shown in Figs. 5.41 and 5.42. Critical signals coming from a focalization failure or malfunctioning valves require a complete and fast beam stop, these signals activate the FBI inhibition. Wrong level of vacuum requires also the closing gate valve system (GVOI).

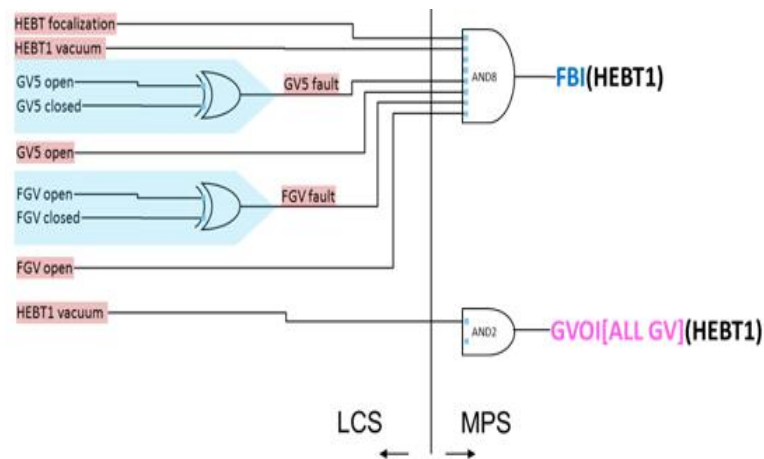


Figure 5.41: HEBT MPS logical diagram

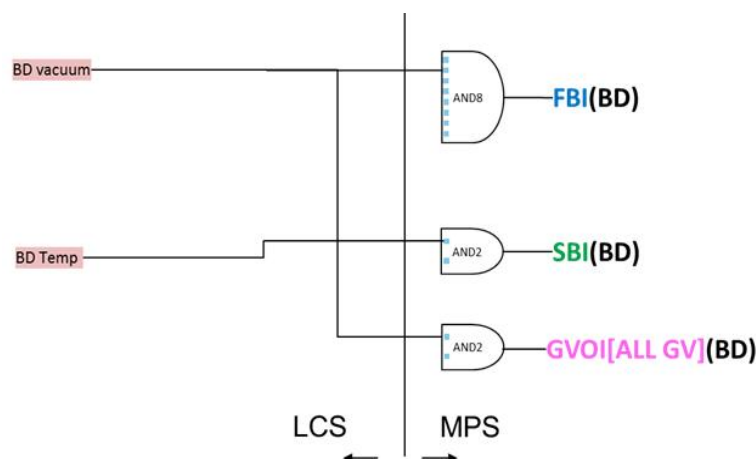


Figure 5.42: BD MPS logical diagram

### 5.9.4 HEBT and BD LCS architecture

In Fig. 5.43 HEBT LCS architecture is shown. The equipment layer has two main parts, first, instrumentation for cooling, pumping and vacuum, and second, power supplies for the magnets. Regarding to the instrumentation and using the above mentioned criteria, the control is PLC based. The solution uses a Windows embedded PC, on the intermediate level, running a combination of commercially available OPC server. This alternative ensures a rapid and effective treatment of analog and digital signals that do not require complex operations. Furthermore, this solution allows to turn over the required signals to the EPICS Channel Access by a configuration that is highly reusable in other PLC based systems, more details of this integration are given in section 5.4.6.3.

Power supplies are controlled with embedded PC Linux settled in the intermediate layer following the same StreamDevice solution for the EPICS device support. EPICS platform and StreamDevice support have been successfully tested on a PC NEXCOM NISE 3500. This PC is Intel Core i7/i5 Fanless System with VGA, DVI-I, eSATA and one Expansion Slot. It is designed for a wide range of applications which demand intense work for extended periods of time with high reliability. There are several choices for controlling power supplies but not many are able to fit with EPICS Channel Access. A serial control based on an EPICS generic device support such as StreamDevice is a quite standard and cheap solution. The only prerequisite to achieve this solution is that these power supplies have a serial port communication.

The upper layer, the EPICS supervision one, corresponds with the Central Control System (CCS), it has main human-machine interfaces. It is a Linux PC running Control System Studio (CSS) and other top level EPICS applications for supervision.

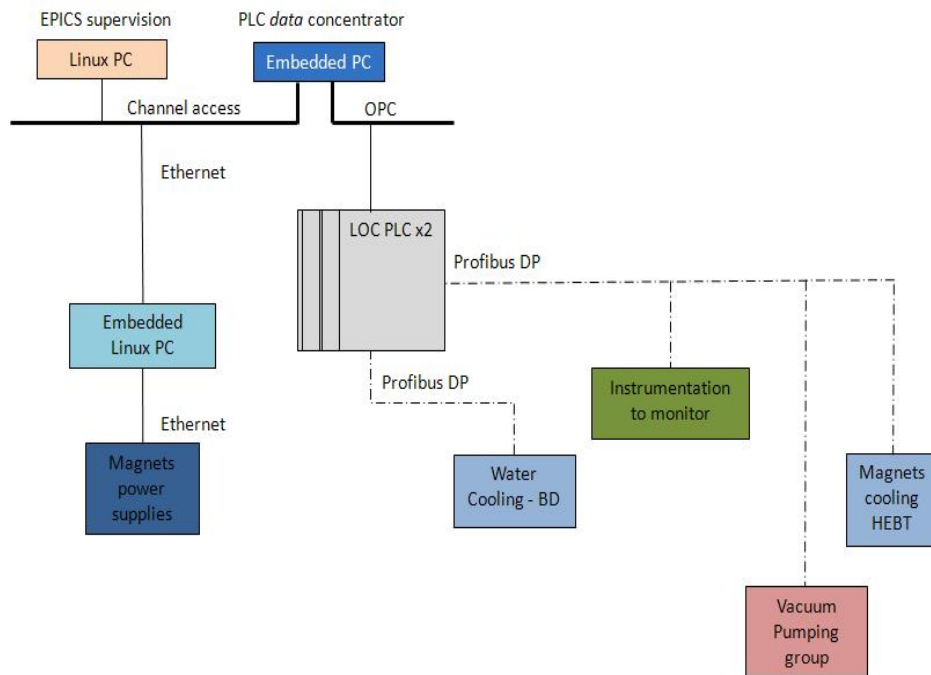


Figure 5.43: HEBT and BD LCS Architecture

## 5.10 Radio Frequency (RF) LCS

### 5.10.1 RF subsystem description

The RF power system contains all the equipment necessary to generate the required conditioned RF power to feed the LIPAc cavities. These cavities require 18 RF power inputs at 175 MHz (each one, fed by one RF amplifying chain) distributed as follows: eight 200kW inputs for the RFQ, two 16kW inputs for the MEBT and another eight 105kW inputs for the SRF Linac [119]. Each RF module, see Fig. 5.44, is composed of two chains. Therefore, there are 9 RF modules for 18 amplifying chains.

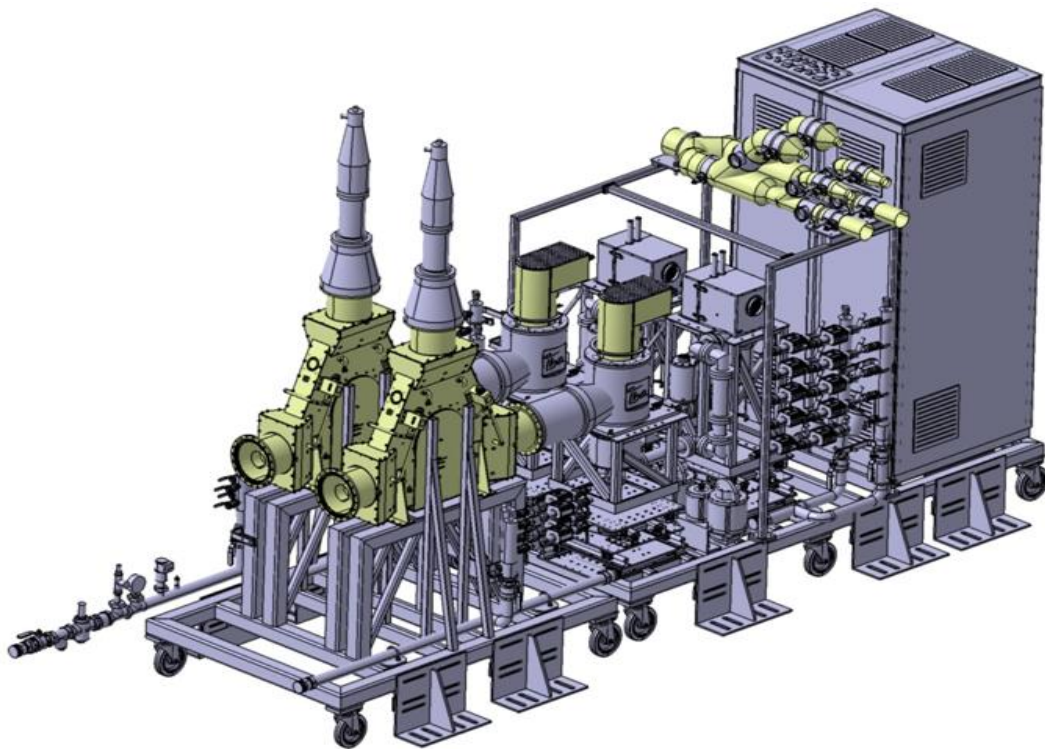


Figure 5.44: RF module scheme. Two amplifying chains, one module

The first stage of the RF chain (pre-driver) is a 400 W commercial amplifier using solid state technology. The second stage (driver) is an electron tube amplifier which integrates a tetrode in a 175 MHz cavity. It is designed to reach a power of 16 kW in CW mode. And the third stage (final amplifier), that integrates also a tetrode, is optimized to provide a RF power up to 230 kW in CW mode, an schematic overview of the RF system amplifying chain is showed in Fig 5.45.

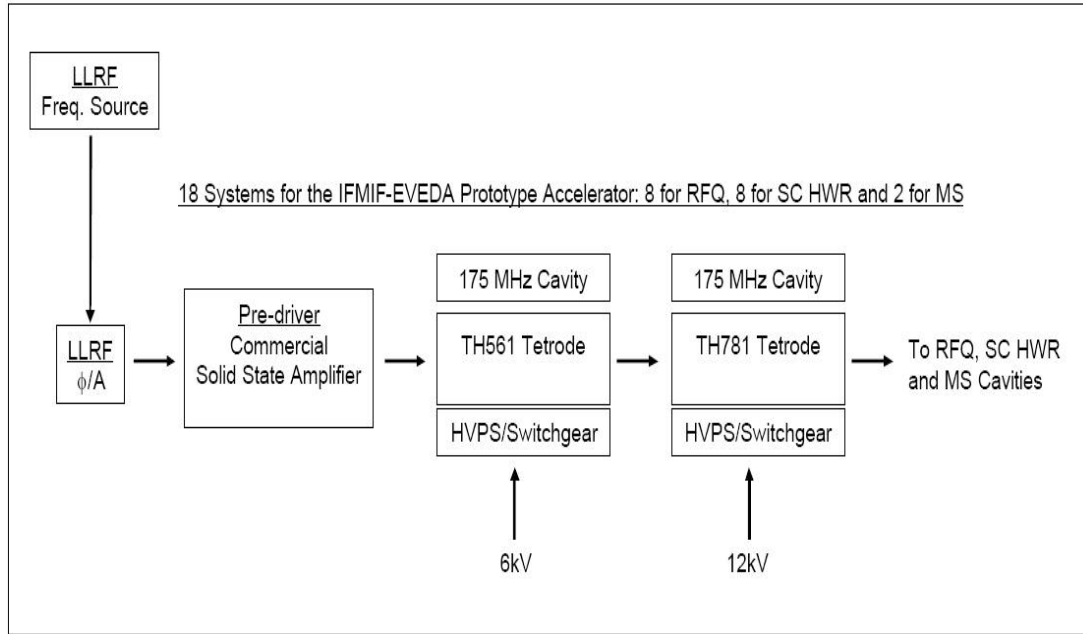


Figure 5.45: RF power system amplifying chain

The main challenge of the RF power system is to provide the required RF power to LIPAc. The quality of the delivered RF to the accelerator cavities is controlled within  $\pm 1$  degree in phase and within  $\pm 1\%$  in amplitude using a Low Level RF (LLRF) system. The RF signal distribution provides all of the RF chains with a stable source. Another aim is to validate its design to be applied for the future IFMIF accelerator. Main performances of the complete RF system are summarized in 5.9.

Table 5.9: RF power system main performances

RFPS main parameters		
Requirement	Target value	Comment
Frequency	175 MHz	Frequency synthesizer as master oscillator
Bandwidth	$\pm 250$ KHz	-1dB bandwidth
Phase Stability	$\pm 1$ degree	Closed loop
Amplitude Stability	$\pm 1\%$	Closed loop
Power Linearity	1%	Closed loop
Output RF Power Range	Up to 200 kW	
Operating Modes	Pulsed mode/Continuous mode	
RF Chains for the RFQ	8 units	
RF Chains for the SRF LINAC	8 units	
RF Chains for the MEBT	2 units	
Transmission Lines for RFQ	Coaxial 9" 3/16	
Transmission Lines for SRF LINAC and MEBT	Coaxial 6" 1/8	
RF FA Anode PS Maximum Output Power	400 kW	
RF FA Anode PS Accuracy	$\pm 2\%$	(including ripple)
RF FA Anode PS Emergency Stop	$< 20$ ms	
RF Power Emergency Stop	$< 10$ $\mu$ s	
Breakers		
Electrical network	6.6kV, 50Hz, 3 phases	
Rated Voltage	6.6kV	
Rated Current	Up to 60A	
Breaking current capacity	Up to 20kA	
Transformer		
Input network	6.6kV, 50Hz, 3 phases	
Input Voltage	6.6kV	
Output Voltage	500V	
High voltage power supply		
Maximum output voltage	13 kV	
Maximum output current	45 A	
Maximum DC output power	400 kW	
Switching-Off time	Less than 20 ms	
Voltage accuracy	Better than $\pm 2\%$	
Operation Modes	Continuous and pulsed	
End RFPS main parameters table		

### 5.10.1.1 RF subsystem functional scheme and description

The RF power required along the LIPAc accelerator is generated by a set of RF chains powered by RF final amplifier anode power supplies. The initial RF wave is created by a low level RF system (A, see Fig. 5.46) insuring flexible control and then is amplified by a chain made of a solid-state pre-driver (B) and two successive tetrodes (C and D).

The circulator (E) directs the forward power to the coaxial lines connected to the accelerator cavities (7) and the reflected power to a water-cooled load (6).

The electric power required to drive the anode of the final tetrode is passing through breakers (1), step-down transformers (2) and harmonic filters before being conditioned by the HV power supplies (3, see Fig. 5.46).

A water-cooling system (5) extracts the energy from the HV power supplies, the driver and final amplifiers, the circulators and the loads. Also, a forced air system (4) is used to cool down some specific components of the driver and final amplifiers, see Fig 5.46.

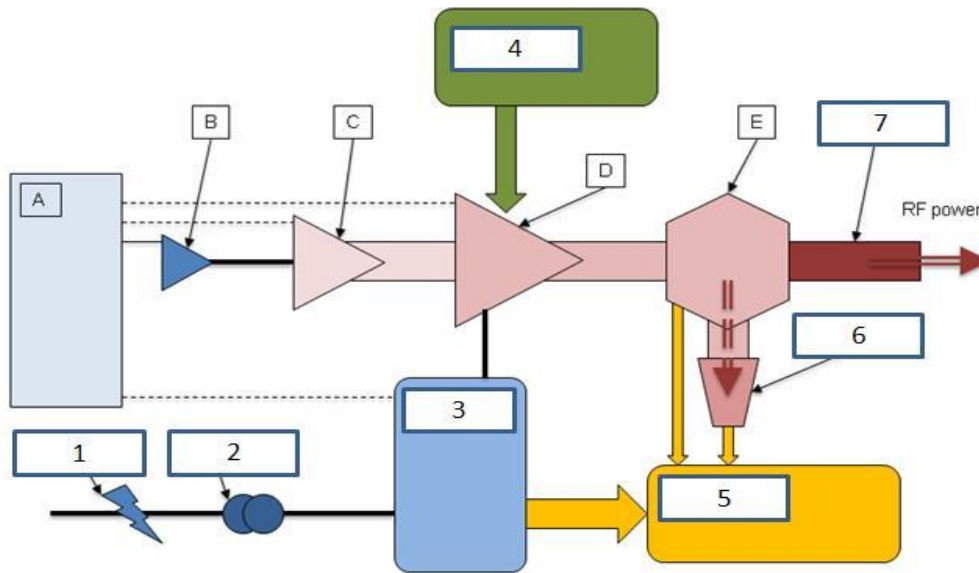


Figure 5.46: Functional scheme of the RF power system

### 5.10.2 RF LCS requirements and design

In order to accomplish the mentioned requests of the RF power system, each RF chain is comprised of the following elements that must be controlled by the LCS:

- Pre-driver.(Solid state amplifier). The RF pre-driver amplifier consists of an air cooled 500W continuous wave solid state amplifier at 175MHz with a  $\pm 1\text{MHz}$  typical bandwidth. It amplifies the RF signal in a balance power amplifier stage. The output of the amplifier is then connected to the input port of a power circulator. The amplifier



can be controlled in local mode using the control panel, display panel and LEDs or in remote mode via Modbus IP, Telnet, HTTP and SNMP protocols.

- Driver amplifier. The RF Driver Amplifier is a 16kW CW amplifier at 175 MHz based on the TH561 tetrode and TH18526C cavity. The tetrode is powered by four different power supplies, one for each terminal (filament, control grid, anode and screen grid). Thus, elements to control in the driver amplifier are power supplies and cooling systems.
- Final amplifier. The RF Final Amplifier is a 230kW CW amplifier at 175MHz based on the TH781 tetrode. The tetrode is powered by four different power supplies, one for each terminal (filament, control grid, anode and screen grid). In the 105 kW RF chains, the anode power supply is shared by the two chains. Thus, elements to control in the final amplifier are again power supplies and cooling system.
- Power supplies for amplifiers. Power supplies needed to feed the amplifiers. They will be controlled with a programmable logic controller (PLC).
- Circulator load. The circulator load shall be able to dissipate as heat the reflected power entering at the circulator output. This reflected power returning from the accelerator cavities under the different operating conditions will be driven by the circulator to its load port. This dissipated heat in the circulator load will be extracted by the water cooling system. An embedded cooling control system is associated to the circulator load. Status of this embedded system will be noticed by a PLC based system.
- Circulator. circulator is designed to protect the RF Final Amplifier from the reflected RF power, as this power will overheat, damage or even destroy the tube based amplifier leaving unusable the whole amplifying chain. The circulator is equipped with an arc detector view port connector. The view port allows the connection of a high sensitivity arc detector system via a low loss fiber optical cable. Using the interlock function for the LLRF, the circulator and the entire RF amplifying chain can be protected from damage due to unwanted arcing or voltage breakdown generated by moisture or contamination inside the coaxial line. The circulator will be temperature controlled to optimize its impedance in any condition. Due to the RF power (forward and reflected) the circulator losses generate heat that affects the ferrite magnetic field as the temperature changes. The magnetic field generated by the ferrite can be slightly changed applying some current to the circulator internal coils. This coils current is controlled by the temperature compensating unit (TCU) adjusting the magnetic field to minimize the reflected power by the circulator to the RF final amplifier. In this way the matching between the RF final amplifier and the circulator is always optimized independently of the circulator temperature. These control tasks are carried out by embedded proprietary systems. Following the same criteria, the status of this embedded system will be noticed by a PLC based system.
- Water and air cooling for amplifiers, circulator load and circulator. Cooling systems used to keep these devices at optimum operating conditions, will be controlled also with programmable logic controller. Water Cooling System is the water primary circuit that provides the required water flow (with a certain temperature, pressure and water quality) and also dissipates the necessary thermal power for all the RF power system

equipment. This cooling system is a closed circuit using deionized water, including the needed water purification equipment.

- Amplifiers Protection System (PSYS). Operation of protection system is based on voltage and current sensors measuring all relevant voltages and currents. According to measured voltages and currents and their time behavior, protection system can give order to crowbar devices or power supply to switch off RF input and DC power supply of driver and final amplifier. This subsystem is in charge of detecting dangerous situations in the RF module tetrodes, and of reacting in due time to avoid critical damage in those components. Case such a situation is observed, the protection system will immediately power off the failing RF chain (or both chains, in 105 kW RF modules). PSYS is controlled by a programmable logic controller and it has direct communication with the Channel Access.
- HVPS. HVPS which contains all the electrical and electronic equipments necessary for the power conversion from low voltage AC input to high voltage DC output, including a crowbar and a protective resistor. They have their own control and protections.
- Master Oscillator, see section 6.2 for more details. It is a commercial signal generator which provides and distributes a 175Mhz signal which is amplified to 230kW at the final amplifier output.
- Low level radio frequency (LLRF) system, see section 6.2 for more details. The LLRF system mainly controls the amplitude and phase voltage of the 18 RF chains of the accelerator (8 for the RFQ, 2 for MEBT and 8 of SC HWR), providing the RF drive or input to the RF amplifiers. This system will control as well the resonance frequency of the cavities. The SRF Linac and MEBT cavities will be adjusted modifying their shape moving a tuner and a plunger respectively, inwards or outwards the cavity body (mechanical tuning). The RFQ cavity will be kept in resonance adjusting its temperature (temperature tuning).

Most of RF control (cooling, measures of temperature and status of the embedded systems) is achieved by means of a PLC, and an OPC server to communicate with EPICS. They are mostly analog and rapid signals and they do not need specific algorithms of processes. On the other hand, the PSYS, beside having a direct control on the part of the PLC, has also a direct communication with EPICS's Channel Access. The protection system is connected to Channel Access through nine pins serial Sub-D connector. This communication is managed using EPICS StreamDevice support, that means that PSYS is controlled by sending and receiving strings. Hereby, the PSYS can send and receive interlock and inhibit signals to and from the LCS. Hereby the PSYS can send and receive signs of interlock and of inhibit to and from the own(proper) LCS.

To automatically start the RF chains, it is necessary to execute a thread following a state diagram. This process is carried out by means of State Notation Language (SNL), that provides a simple yet powerful tool for programming sequential operations in a real-time control system. This SNL program is executed in a Linux PC.

### 5.10.3 RF system MPS

In the design of each LCS, there are several signals which should go to MPS system. These signals come from certain elements which are essential for the proper functioning of the machine and whose malfunction can have disastrous consequences in seconds. The space available for the reception of the MPS signal space is finite, so the signals can be summed up as far as possible using logic gates. Some signals in the RF LCS that will inhibit the operation of the beam by means of BRTZ, FBI or SBI, see 5.4.5 for more details, can be seen in Fig. 5.47. Since RF is a system that widely interfaces with other subsystems, interlock alarm coming from any part of a subsystem requires also stopping the RF power, see section 6.4.4.9, at the same time it is activated the FBI inhibition and the closing valve system (GVOI) if it is a vacuum fault.

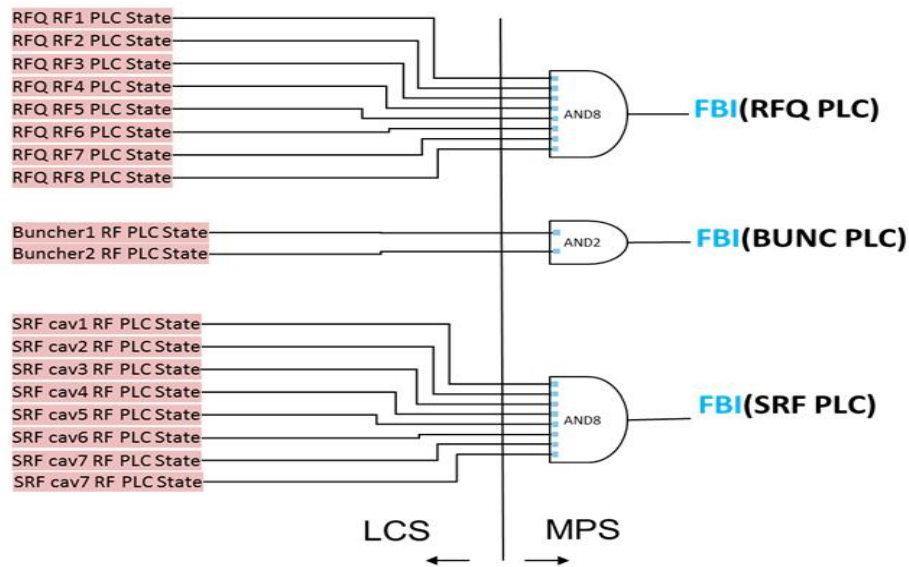


Figure 5.47: RF MPS logical diagram

### 5.10.4 RF LCS architecture

RF LCS development has been mainly developed in the framework of the thesis, both the LCS architecture design shown in Fig. 5.48 and the RF MPS configuration explained above. This control architecture is repeated in each of the 9 RF modules, one control module per two amplifying chains. This architecture has two main control elements, one is the PLC and the other is the LLRF. The PLC controls all the equipment level except for the master oscillator, namely, water and air cooling, embedded systems, amplifiers, PSYS, power supplies and high voltage power supplies (HVPS). Using the above mentioned criteria, for the communication between Siemens PLCs and EPICS, many solutions are available. The communication based on the OPC protocol is used, Fig. 5.18. This protocol uses Microsoft's COM and DCOM technologies to enable applications to exchange data using a client/server architecture. The solution uses a Windows embedded PC running a combination of commercially available OPC server and server packages with a special EPICS device support. Thus, this alternative

ensures a rapid and effective treatment of analog and digital signals that do not require complex operations. Furthermore, this solution allows to turn over the required signals to the EPICS Channel Access by a configuration that is highly reusable in other PLC based systems, more details of this integration are given in section 5.4.6.3.

The upper layer, the EPICS supervision one corresponds with the Central Control System (CCS), it has main human-machine interfaces. There is a Linux PC running Control System Studio (CSS) and other top level EPICS applications for supervision. This Linux PC is also executing an State Notation Language (SNL) program, it is a domain specific programming language that smoothly built on EPICS base. As explained before, this program is used to automatically start the RF chains following a state diagram. This procedure must be done in the RF system due to the high number of devices, in order to power the system up incrementally.

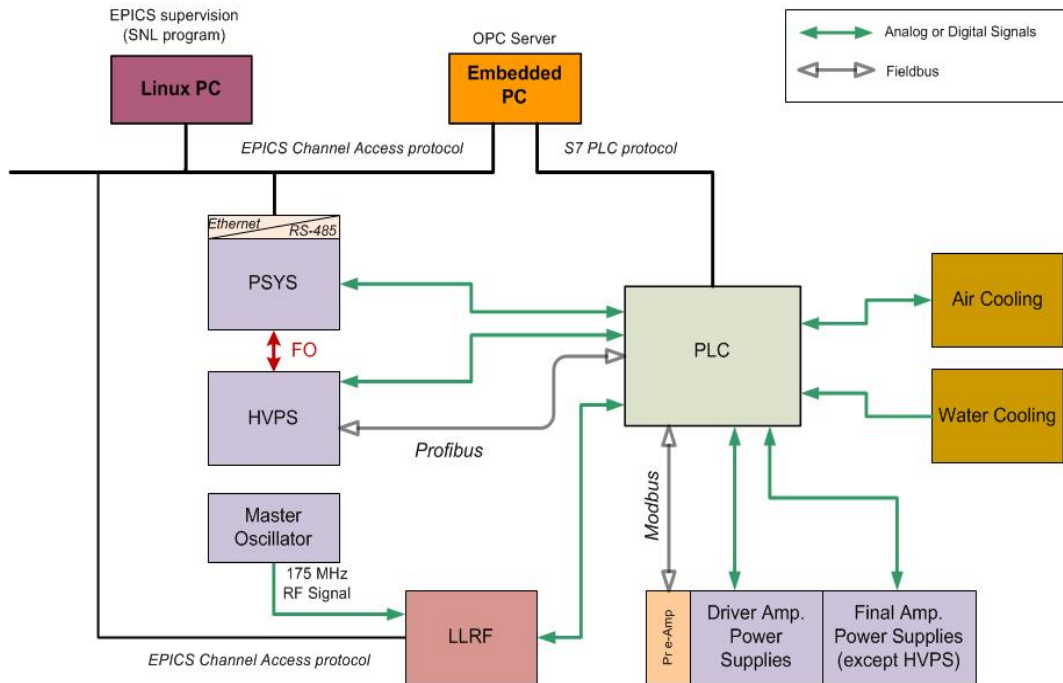


Figure 5.48: RF power system LCS architecture

## 5.11 Beam instrumentation (BI) LCS

### 5.11.1 BI subsystem description

BI subsystem must warranty the successful operation of the accelerator from commissioning phases of RFQ, MEBT, SRF and HEBT, to the full power operation. Hence, the main objective is to provide all necessary information to properly transport and accelerate the beam from the source to the BD, then, to fully understand and measure all beam characteristics.

Most of the diagnostics are concentrated inside of the Diagnostics Plate (DP or D-plate). DP is a movable set of diagnostics that is placed downstream from the SRF Linac, in the HEBT. During the first commissioning phase it will be placed at the exit of the MEBT. Main parameters of the beam will be measured in the DP, e.g. current, phase, beam position, transverse profiles, mean energy, emittance measurements, micro losses, energy spread, etc.

The layout of the beam instrumentation proposed for LIPAc from the MEBT to the BD is shown in Fig. 5.49. Beam loss monitors (BLoMs), Current transformers, beam position monitors, micro-losses monitor, slits, Secondary Emission Monitor (SEM) Grids, non-interceptive profilers and transverse halo monitors are present along the accelerator.

Beam measurements play a critical role for the LIPAc due to its uncommonly high beam current and high beam power. But that also makes difficult the installation of certain measurement devices. A global measurement strategy is thus necessary to clearly decide between the different measurements categories.

Except for some specific devices, interceptive ones, most of the beam diagnostics, must be able to provide information for pulsed and continuous beams as well, from minimum to maximum beam current. BI main parameters are listed in Tab. 5.10.

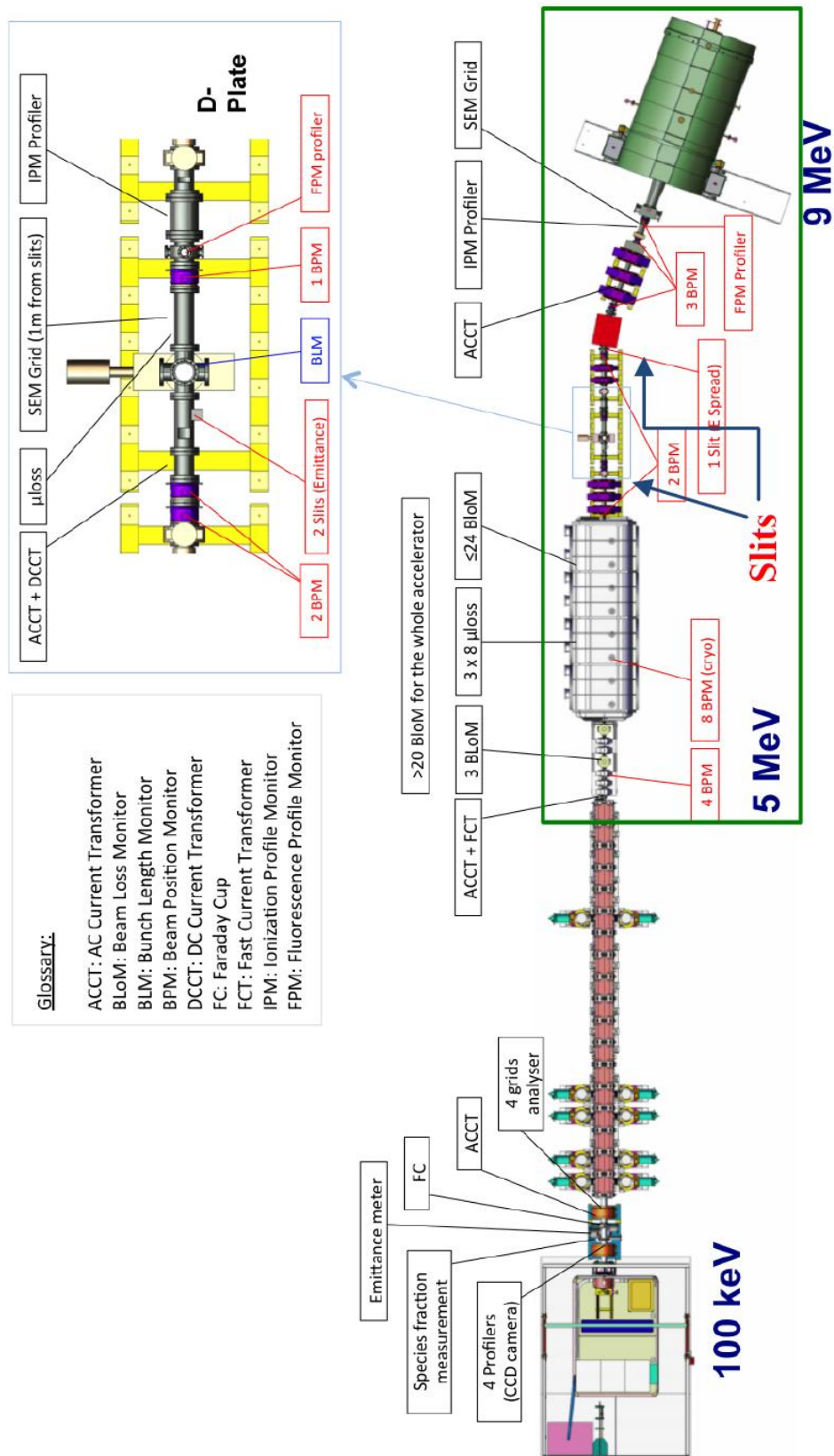


Figure 5.49: Layout of Beam Instrumentation along the accelerator [11] [12]

Table 5.10: Requirements and target values for the BI

Beam Instrumentation main parameters		
Requirement	Target value	Comment
<b>Beam Characteristic</b>		
Species	$D^+$	$H^+, H_2^+$
Maximum beam current	125 mA	
Beam energy	5 to 9 MeV	
Maximum beam power $P_{max}$	1.125 MW	
RF frequency	175 MHz	
<b>Current transformer</b>		
ACCT	Precision: 0.15 mA	3
DCCT	Resolution: 1mA	1
FCT	$BW > 0.5GHz$	1
<b>MEBT BPM</b>		
Number	4	
<b>Cryogenic BPM</b>		
Number	8	
<b>Diagnostic plate (D-plate) BPM</b>		
Number	3	
<b>HEBT BPM (w/o Dplate BPMs)</b>		
Number	5	
<b>Beam Loss Monitor</b>		
Number	Sensitivity $> 10^{-18}$ C/ $\gamma$	$> 30$
<b><math>\mu</math>-losses</b>		
Number	TBD	24
<b>Fluorescence Profiler Monitor</b>		
Number	2 pairs	
<b>Beam Transverse Profile Monitor</b>		
Number	2 pairs	
<b>Secondary Emission Monitor Grid</b>		
Number	2	X&Y wires
<b>Sliding Slits for EM and ES</b>		
Number	3	
<b>Residual Gas Bunch Length Monitor / Fast Faraday Cup</b>		
Energy	2.5 MeV	
current	70 mA	
Macro-bunch	100 $\mu s$	1 Hz
Micro-bunch	300 ps	Hz
<b>End HEBT and BD main parameters table</b>		

### 5.11.2 BI LCS requirements and design

BI LCS development for the BPMs, FPMs and slits has been mainly made in the framework of the thesis, specifically the architecture design shown in Fig. 5.51 and the derived EPICS applications, besides the MPS configuration. There is instrumentation for diagnostic along the whole accelerator. In this section, beam instrumentation downstream the RFQ is considered, other instrumentation for diagnostics located in the injector have been described in the injector LCS part, see section 5.5, and bunch length monitoring for the RFQ has been described in RFQ LCS section 5.6. Accordingly, following devices must be controlled:

- Ionization Profile Monitor (IPM). The goal is to measure the transverse beam profile. One IPM acquires a single profile either horizontal or vertical. The resolution of the monitor is around 1mm and the data must be acquired at a 10Hz repetition rate. Two IPMs are located in the D-Plate (2x80 channels, one vertical and one horizontal) and another one upstream of the BD (128 channels).
- Beam Loss Monitor (BLoM). The goal is to measure along the accelerator (from the RFQ to the HEBT) the particle losses for machine safety. In case of unacceptable beam loss, an interlock signal is sent to the MPS independently of the LCS. A number of 20 monitors is planned. An acquisition rate of 10 Hz is needed.
- $\mu$ -Loss Monitor ( $\mu$ LoM). The goal is to have a sensitive measurement of low losses in order to tune accurately the Linac. A number of 24 monitors will be installed inside the cryomodule of the SRF Linac. As the measurement is slow, an acquisition repetition rate of 1Hz only, for the 24 channels is needed. The method of measurement will consist of 3 discriminators with variable thresholds and counters. There are 3 discriminator levels for each channel.
- Beam Current Monitors (CT). The goal is to measure the beam current from 0.1 msec pulsed mode to CW mode with a dynamic range between 1 to 150 mA. 3 different kinds of monitors are planned:
  - 3 ACCTs for MEBT, D-Plate and HEBT.
  - 1 Direct Current Transformer (DCCT) for D-Plate. An acquisition rate of 1MHz is needed for these 4 channels.
  - 1 Fast Current Transformer (FCT) for MEBT. For this monitor, a measurement with an oscilloscope is foreseen. It will be used to analyze the RF beam structure. For this purpose a bandwidth of 1GHz is needed.
- SEM Grids. The goal is to have a beam profile measurement at low duty cycle in case of IPM measurement is not sensitive enough. These diagnostics are mostly required for beam commissioning. One SEM grid is included in the D-Plate and another one before the BD.
- Beam position monitors (BPMs). The beam position and phase monitors will become one of the key devices for the beam commissioning and operation of the accelerator. They will provide the variation of the beam centroid in the transverse plane (position)



and the longitudinal plane (phase). The BPMs will be distributed along the transport lines MEBT (4) and HEBT (2+3) and superconducting accelerating sections (8). Furthermore, the BPMs located in the D-plate (3) will be dedicated to carry out energy measurements. This information is crucial for the tuning of the cavities and a proper validation and characterization of the output beam in each beam commissioning stage.

- Fluorescence profile monitors (FPMs). The objective is to develop a non-interceptive beam transverse profiler based on the residual gas fluorescence originated by the beam-gas interaction. FPMs (2 in HEBT, 2 in D-plate) could be used as well for the emittance measurements with quadrupole scans.
- Slits. As part of the diagnostics equipment, movable slits are used for the emittance measurement of the beam. The device is placed at the diagnostic plate. Another slit is located in HEBT, just before the dipole.
- Vacuum. It consists of 4 pumping units, 4 valves and 4 gauges. An additional valve is installed at the end of the D-plate.

Once the devices and their performance used to diagnose have been explained, several solutions are developed to control and to interface them due to the variety of devices and the interfaces/protocols they support:

#### **Control of the IPM.**

- HEBT IPM X (128 signals): 1 ICV150 VME board equipped with a 16 bits ADC +/- 10Volts and 32 multiplexed inputs. It provides a maximum acquisition rate of 30,000 acquisitions/second. 2 ICV110 slave boards with 48 multiplexed inputs. The data path between the master (ICV150) and the slaves (ICV110) is done through the P2 I/O lines of the VME.
- DPlate IPM X and Y (80 signals each): 2 ICV150 VME board equipped with a 16 bits ADC +/- 10Volts and 32 multiplexed inputs. It provides a maximum acquisition rate of 30,000 acquisitions/second. 2 ICV110 slave boards with 48 multiplexed inputs. The data path between the master (ICV150) and the slaves (ICV110) is done through the P2 I/O lines of the VME.

For all IPMs management: 1 ICV196 VME board (96 binary input/output signals).

The available acquisition rate gives a scanning rate for the 128 channels (32 + 2\*48 channels) larger than 200Hz. The mode of the acquisition will consist of a permanent scanning of the channels. The signal conditioning module is responsible of the sample and hold functions of the incoming signals when the beam is pulsed. A trigger (beginning of pulse) is provided to the signal conditioning module by the TS.

The ICV196 board is used to configure the two 64 integration boards:

- 5 outputs for the integration time and type and the polarity.
- 1 output for reset of the integration board.

- 1 output for requesting the integration.
- 1 input for the *beam in on* signal.

**Control of the BLoM.** The electronics will provide a signal for the MPS and the injector thanks to two thresholds. These signals used to switch off the beam are not part of the control system. On the other hand the integrators similar to the ones developed for IPMs, will be monitored by an ICV150 VME module and managed by an ICV196.

The programming of the thresholds and gains for the discriminators will be done by the MCP4728, an electronic component composed of four digital analogue converters. It is programmable by I2C protocol. A gateway which allows the conversion from I2C protocol to RS232 protocol is used and then easily interfaced with EPICS.

**Control of  $\mu$ -Loss Monitor.** This solution consists of measuring the counting (scalers) rates for 3 thresholds of deposited energy in the diamond. In this, a SIS3801 card with an available EPICS driver is used.

**Control of beam current monitors.** For the acquisition of the signals, a 8 channels fast acquisition is provided composed of:

- 1 ICV108 VME board acquisition controller
- 1 ICV178 VME board with 8 ADCs 16 bits +/- 10Volts

**Control of SEM grids.** The control (in/out) and the profile readings are done by a dedicated controller through the MODBUS-TCP protocol on Ethernet. The SEM grids controller is connected with the second Ethernet port of the CPU.

**Control of BPMs.** For BPM electronics interfacing a solution based on the same cPCI boards (Lyrtech) as the LLRF was tested taking advantage of the previous experience gained in order to get a working implementation of this system. This choice has suitable options with ADCs from 14 to 16 bit with sampling rate up to 100 Msamples/sec. The data will be available at 10Hz which is convenient for monitoring and for beam optimization programs. The information for each BPM consists of X,Y positions and phase. The computation of the data is performed by the FPGA included in the acquisition electronics.

**Control of FPMs.** A solution based on a Vertilon data acquisition system has been chosen. This solution is widely used for data acquisition of signals from PMTs. The Vertilon system has a USB port for connection to any external system. Vertilon provides a Labview based solution to interface its system. A High voltage control for the PMT is required (HV enable/disable, HV setting). The Vertilon system has a USB port for connection to any external system. The acquisition system will deliver 64 data points for both FPMs of the D-plate and 32 data points for both FPMs of HEBT. The data will be available at 10Hz.

**Control of Slits.** The D-plate slits will be operated with the same solution than for MEHT buncher (control of 2 stepping motors). For these slits, a cooling system is required and a thermocouple will be monitored. For the HEBT slit, a simple in/out command is required.

**Control of vacuum.** This system is standardized with the equivalent vacuum systems used for MEBT and HEBT, see section 5.9.2.

**Post-mortem acquisition.** To be able to analyze possible beam anomalies after an interlock alarm detection, the BI LCS must provide a way to store permanently (circular buffer) the diagnostics data obtained for a given period of time depending of the diagnostic acquisition frequency and to freeze and transmit the buffer in case of occurrence of a trigger (MPS). Data will be retrieved from the VME systems to a hard disk in order to be analyzed by offline analysis tools. The major challenge is to store data continuously with high rate coming from the fastest diagnostics in term of bandwidth. So, a dedicated acquisition system is used. The only exception concerns IPMs where it is believed that this low flux of data can be managed locally with a dedicated software without additional hardware. The post-mortem VME hardware is composed of standard elements as already used for beam diagnostics fast acquisition. The configuration consists of one ICV108 controller and four ICV178 acquisition modules (4 CTs + 24 BLoMs). The ADAS VME board ICV108 will be connected to 4 CTs and 24 BLoMs. The acquisition frequency for all channels will be 1MHz maximum.

In BI LCS, several signals are used to describe the status and the operation of devices and elements explained above through the adopted control solutions. Each one of these signals must correspond with an EPICS PV. To achieve this equivalence, it is necessary to implement a device support which must be able to understand each device and to communicate with the EPICS Channel Access in order to write and read all process variables, that is, all signals.

In Tab. 5.11 several examples are shown, one example of a signal from each device is provided. Table fields have been defined in previous sections.

### 5.11.3 BI MPS

In the design of each LCS, there are several signals which should go to MPS system. These signals come from certain elements which are essential for the proper functioning of the machine and whose malfunction can have disastrous consequences in seconds. The space available for the reception of the MPS signal space is finite, so the signals can be summed up as far as possible using logic gates. Some signals in the BI LCS that will inhibit the operation of the accelerator by means of BRTZ, FBI or SBI inhibition methods, see 5.4.5 for more details, can be seen in Fig. 5.50. The status of the beam is always a crucial information, both working in low duty cycle or maximum power operation, any kind of alarm coming from the beam condition or from the beam loss monitors must immediately stop the operation, using BRTZ or FBI inhibition for low duty cycle or high duty cycle respectively.

Table 5.11: Examples of PVs for the BI LCS

Signal description	Record type	Process variable name	EPICS device support
BPM. Transverse plane beam position readback	Analog input	BI:BPM1:PosRdbk	AsynPortDriver
BPM. Longitudinal plane beam position readback	Analog input	BI:BPM1:PhasRdbk	AsynPortDriver
Slit Stepper motor. Set stepper motor position	Analog output	BI:SlitSM1:SetPos	EPICS OPC Server/Client
Slit Stepper motor. Readback stepper motor position	Analog input	BI:SlitSM1:PosRdbk	EPICS OPC Server/Client
Vacuum DP. Status DP vacuum level in pump1	Binary input	BI:DP_Pump1:VacStat	StreamDevice
FPM. Beam profile readback on X axis	Analog input	BI:FPM1:PosxRdbk	Labview to EPICS
FPM. Beam profile readback on Y axis	Analog input	BI:FPM1:PosyRdbk	Labview to EPICS

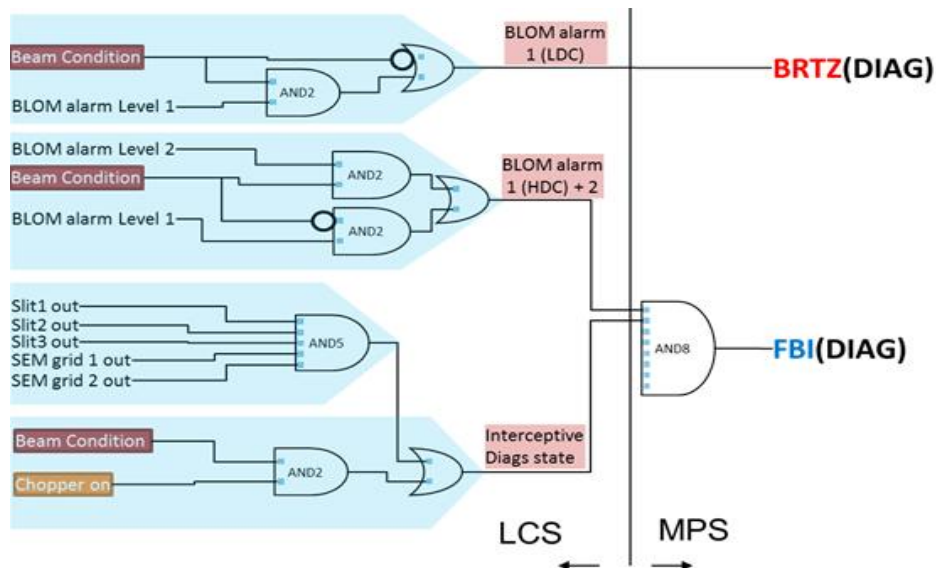


Figure 5.50: BI MPS logical diagram

#### 5.11.4 BI LCS architecture

Two different parts of the BI LCS architecture can be observed, first one is showed in Fig. 5.51. This part has slits, slits water cooling and vacuum of the D-plate as elements that are controlled using a PLC. With respect to the slits stepper motors, the proposed control solution is the same as the one explained in section 5.9.2. For the communication between Siemens PLCs and EPICS, many solutions are available but following the above mentioned criteria, the communication based on the OPC protocol is used on the intermediate layer, where the IOC is launched. This protocol follows Microsoft's COM and DCOM technologies to enable applications to exchange data using a client/server architecture. The solution uses a Windows embedded PC running a combination of commercially available OPC server and server packages with a special EPICS device support. Thus, this alternative ensures a rapid and effective treatment of analog and digital signals that do not require complex operations. Furthermore, this solution allows to turn over the required signals to the EPICS Channel Access by a configuration that is highly reusable in other PLC based systems, more details of this integration are given in section 5.4.6.3.

Another control solution presented in Fig. 5.51 is the FPM. FPMs need a Linux embedded PC in the intermediate layer to manage the Vertilon system. This system communicates by means of serial port with the Linux PC, where the EPICS IOC is launched. To interface Vertilon system with the EPICS Channel Access, StreamDevice is used. As explained before, it is a generic EPICS device support for devices with a *byte stream* based communication interface. The criteria followed to chose this solution is the same as in power supplies.

And finally, for the BPMs, a Linux cPCI system is chosen. Due to the BPMs high acquisition needs, their control system is based on fast cPCI cards. These boards are managed by a Linux embedded CPU where the EPICS IOC is Launched. A specific device support using EPICS AsynPortDriver is used to communicate the cPCI boards with the EPICS Channel Access.

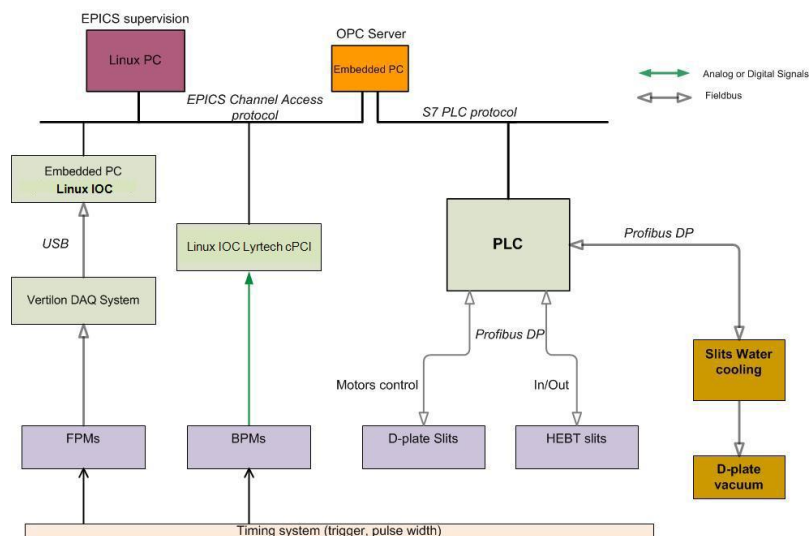


Figure 5.51: BI LCS architecture

The timing signals sent to the source and diagnostics acquisition system are generated by the timing system.

- Source signal: used to drive the pulsed mode of the RF generator. It consists of a TTL pulse with a variable width from 1msec to 1sec.
- Trigger signal for pulsed acquisitions: used to trigger the acquisition of the fast acquisition system (ICV108/ICV178). It consists of a TTL raising edge, present even in continuous mode in order to provide always a starting point to the acquisitions.

The second part of the BI LCS is mainly composed of 2 VME crates and is showed in Fig 5.52. This division in 2 crates seems advisable to save CPU power and VME bandwidth especially for the fast acquisition. One other advantage of this architecture is the natural logical grouping of monitors:

- VME 1: Post Mortem (BLoMs+CT),  $\mu$ Loss Monitors, Acquisition of BLoMs (11 VME slots)
- VME 2: acquisition of SEM grids, IPMs, and CT. (10 VME slots)

The upper layer for both parts is the same, corresponds with the CCS, it has main human-machine interfaces. It is a Linux PC running Control System Studio (CSS) and other top level EPICS applications for supervision.

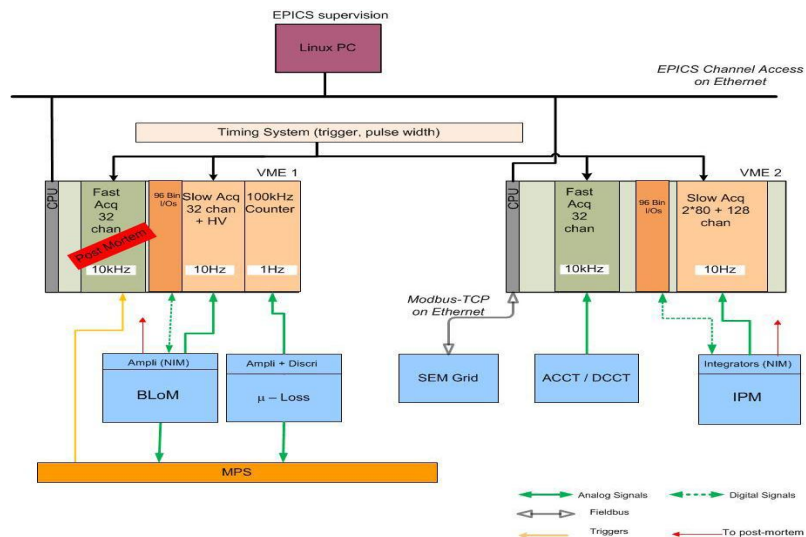


Figure 5.52: BI LCS architecture II

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# 6

## LIPAc Low Level Radio Frequency (LLRF) control system

*¿Por qué sé más de ciertas cosas? ¿Por qué generalmente soy tan listo, tan perspicaz?*  
*Ecce Homo*, Friedrich Nietzsche.

### 6.1 Introduction

As mentioned in previous chapters, low level radiofrequency system belongs to the RF system, accordingly, LLRF control system resides in the RF LCS. LLRF system is a fundamental part of the accelerator that develops a very specific and critical function. It interacts directly with the cavity and with other subsystems, it is able to work in a real-time automatically closed cycle, bypassing the operator and the CCS. These reasons justify that LLRF control system requires an accurate and specific development for the integration with EPICS and the understanding with the others LCSs. Thus, this chapter is devoted exclusively to the LLRF and its control system, of which its software architecture and its EPICS development are considered one of the major contributions of this thesis.

Obviously, to understand the LLRF control system, first, we must attend to what a LLRF means in a RF system, explaining the operation and the modules of a generic RF system, section 6.2. The specific LLRF system for LIPAc is presented in section 6.3, two important aspects are explained here, functionalities and hardware architecture.

In Section 6.4, a complete explanation of the LLRF control system development is exposed. Detailed herein, among other things, the operation of the control system, its architecture and functionalities.

## 6.2 Low level radiofrequency (LLRF) general overview

In order to figure out what a RF system is, it is helpful to first examine its anatomy and then to show its basic components. Generally speaking, a RF system is a device that transforms electrical energy into energy transferred to a beam of particles. More precisely, the energy transformation takes place in three different steps:

1. The transformation of the AC power from the grid (alternate, low voltage, high current) to DC power (continuous, high voltage, low current) that takes place in a power converter.
2. The transformation of the DC power into RF power (high-frequency) that takes place in a RF active element: RF tube, klystron, transistor, etc.
3. The transformation of the RF power into power to a particle beam that takes place in the gap of an accelerating cavity; the efficiency is proportional to the shunt impedance.

An expanded scheme for a RF system is presented in Fig. 6.1; it identifies the five main elements of a RF system, power converter, RF amplifier, the power coupler, the low level RF, and the ancillary systems such as water cooling, vacuum or cryogenic.

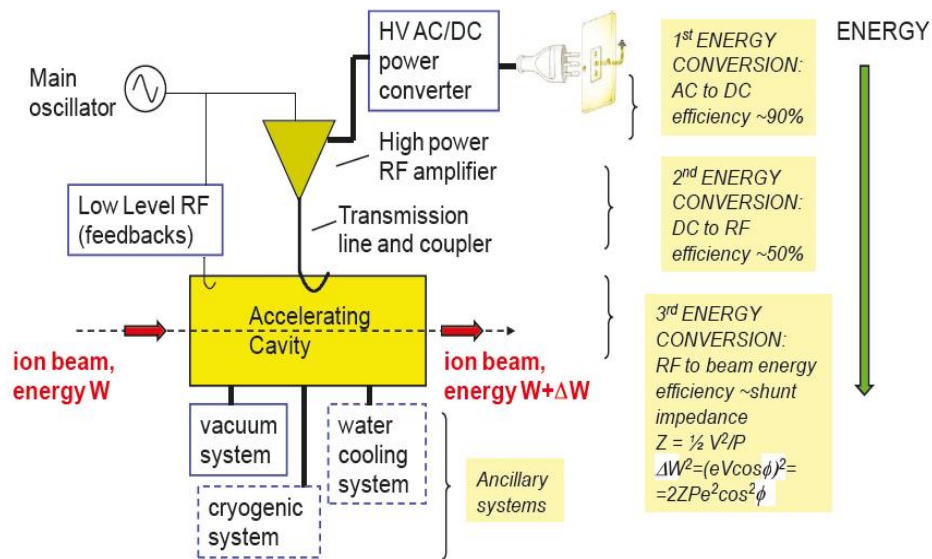


Figure 6.1: Block-diagram scheme of an accelerator RF system [13]

Looking in detail at Fig. 6.1, their main elements can be identified as:

1. The power converter: it is a fundamental part of a RF system not only because it provides the first transformation, but because operating with high voltages it is often one of the main items which represent the latter reliability of the system. Most of the RF systems operate in pulsed mode, and the power converter has to act as a buffer



between the pulsed system and the grid, providing a constant charge to the electrical network. Pulsed power converters are usually called *modulators*.

2. The RF amplifier: used to convert a low-power radio-frequency signal into a bigger signal of considerable power. It is usually optimized to have high efficiency. The conversion takes place by means of an electron beam accelerated by the DC voltage and density modulated at the RF frequency by a grid, by a cavity, or directly by an applied voltage.
3. The transmission line: the power generated by the RF amplifier has to be transported to the accelerating cavity reliably (without arcing), with minimum loss and zero reflection. Rigid coaxial lines, waveguides, or different types of coaxial cable are commonly used for the transmission lines [13].
4. The power coupler: the power transported to the cavity has to be injected into the cavity by a device that needs at the same time to couple strongly the transmission line to the field distribution in the cavity, to provide a way to adjust the matching between the line and the cavity, and finally to separate the vacuum of the cavity from the air of the line.
5. **The Low Level RF (LLRF)**: it is in a sense the brain of a RF system, because at the same time it concentrates and elaborates the flow of information required to guarantee a stable operation and provides the interface with the operators who need to configure the system parameters. A LLRF system is a collection of electronics, slow and fast, analog and digital, which controls the loops from the cavity and/or the beam to the RF amplifiers, it provides constant phase and amplitude of the gap RF field in the presence of perturbations coming from the external environment or from the beam. Main oscillator can be considered as a part of LLRF, which generates the reference operating frequency [13].

### 6.3 LIPAc LLRF system description

LIPAc LLRF system controls the amplitude and phase of 18 three-stage amplifier chains working at 175 MHz (8 chains, up to 200 kW, for the RFQ; 8 chains, up to 105 kW, for the SRF Linac and 2 chains more, up to 16 kW, for the MEBT) [119], providing the RF signal (drive or input) to the RF amplifiers. There are 9 LLRF systems in LIPAc, one LLRF system per RF module, each RF module is composed of two chains, see Fig. 6.2 and see section 5.10.1 for more details of the RF system. The digital signal processing of the LLRF is performed in a field programmable gate array (FPGA)<sup>1</sup> board. FPGA low level control and configuration was previously achieved by [120], employing VHDL<sup>2</sup> and ISE Foundation. The inputs of the FPGA board are undersampled at 100MHz and demodulated into their IQ components. To perform a digital IQ demodulation, the board acquires one sample every 1.75 RF periods. The ADC outputs are then demultiplexed in two channels and the sign of the samples are inverted when required. The relative phase of each signal is compared to the master oscillator phase for the loops adjustments. A software phase shifter is applied to the outputs of the IQ demodulation for precise adjustment of delay lines or phase.

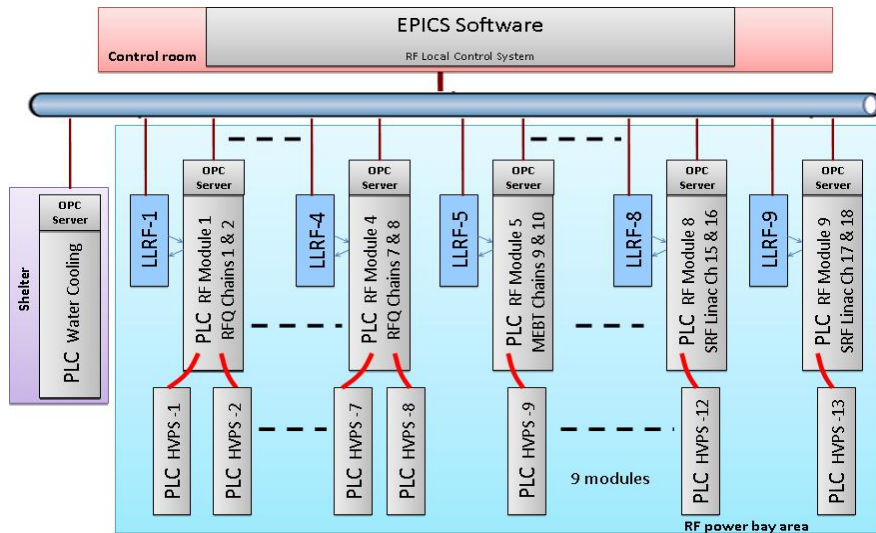


Figure 6.2: One LLRF system per RF module. Each RF module is responsible of two chains

This system also controls the resonance frequency of the cavities modifying their shape. The SRF Linac and the MEBT line cavity body will be adjusted moving a tuner or a plunger, respectively, this is called mechanical tuning. The RFQ cavity will be kept in resonance adjusting its temperature, which is known as temperature tuning.

A fast interlock system will be integrated in the LLRF as well. This safety system will prevent the LLRF sending power to the RF chains in case there is an interlock alarm such as arcing, vacuum peaks, too much reflected power or multipacting.

<sup>1</sup>A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing-hence *field-programmable*

<sup>2</sup>VHDL is the sum of VHSIC (very-high-speed integrated circuits) and HDL (Hardware Description Language)

Main functionalities of the LLRF system can be summarized as:

- To control the resonance frequency of the cavity (tuning).
- To control the amplitude and phase of each cavity field at 175MHz.
- Reception and processing of authorizations to suppress the excitation of the power amplifiers if required. A *fast interlock system* is integrated in the LLRF. This safety system prevents the LLRF sending power to the RF chains in case there is a failure.
- All the I&Q components of the RF signals and other signals involved in the digital signal processing of the FPGA boards are stored in registers of the board to be accessed by the local control system.
- Dialog with the upper level control system.
- Automated conditioning. To adjust the amplitude and the duty cycle of the pulses. These parameters, amplitude and duty cycle, are increased smoothly with an adjustable slope to avoid sudden increases of vacuum pressure.
- Pulsed mode operation. LLRF system is able to work in pulse mode, synchronizing the RF drive with the injection and with the pulse length.
- Automated start up. In order to make easier the recovery of the RF plants from an interlock or a shut down, the LLRF have an automated start up mode.
- Management of the circular buffer of diagnostic signals for post postmortem analysis.

### 6.3.1 LLRF hardware architecture

A modular prototype based on a commercial Compact Peripheral Component Interconnect (cPCI) board (RF module) has been developed to command 2 RF chains. Fig. 6.3 shows a scheme of the LLRF hardware and its main signals. LLRF electronics is composed basically of two main modules:

- Front end modules
- cPCI chassis (host PC + FPGA boards)

The front end is the interface between the RF signals and the digital board. It distributes the RF signals to the digital board and other components when required, and it converts the DC outputs of the digital board to RF. Similar LLRF architectures can be found in [121], [122], [123], [124] and [125].

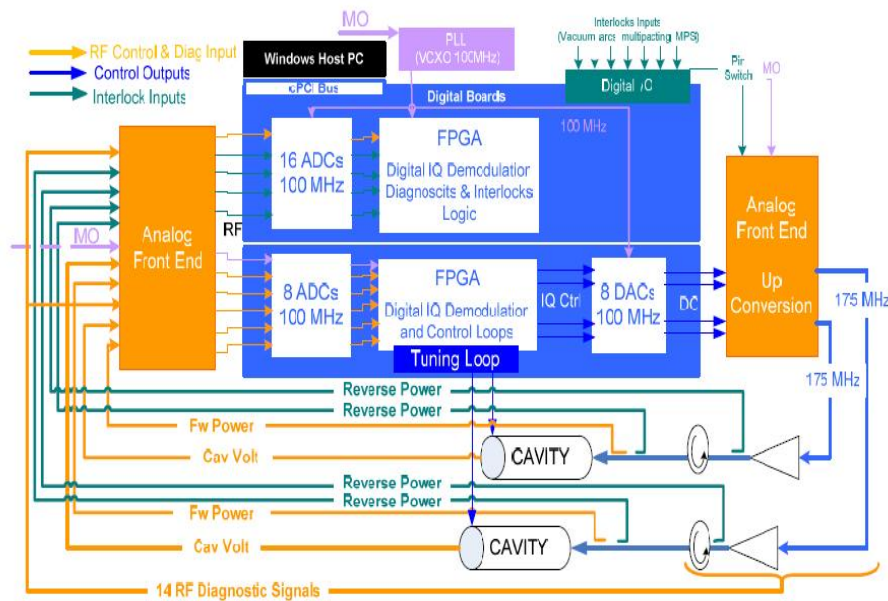


Figure 6.3: LLRF System general overview

### 6.3.1.1 Front ends

There are two front ends. The first one is called *loops front end (LOFE)* and it is used to receive all the signals involved in the loops of the LLRF. The second is known as *diagnostics front end (DIFE)* and it receives all the RF diagnostic signals of the RF plant.

Both front ends allocate the components in a 19 inches standard crate. The LOFE is 3U high and the DIFE is 2U high.

The common components, which are explained below, for both front ends are:

- Bayonet Neill-Concelman (BNC) Test Points

The LOFE also have the following components:

- RF detector for master oscillator (MO) presence detection
- Up conversion front end
- Local timing system: A Voltage-Controlled Crystal Oscillator (VCXO)<sup>3</sup> phase-locked loop<sup>4</sup> (PLL)

<sup>3</sup>It is used for fine adjustment of the operating frequency. The frequency of a voltage-controlled crystal oscillator can be varied a few tens of parts per million (ppm), because the high Q factor of the crystals allows *pulling* over only a small range of frequencies

<sup>4</sup>A Phase-Locked Loop or Phase Lock Loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector

- Pin diode switch

### Test points

There are a number of test points, BNC connectors, in the front panel of this module for diagnostics purposes during tests. The list of the available RF signals through the BNC connectors for the loops is:

- Cavity voltage
- Forward&reversed cavity voltage
- Reversed circulator voltage
- RF drive
- FPGA clock (80MHz)

The test points for the diagnostics RF signals are:

- Forward Amplifier1
- Forward and Reversed Amplifier2
- Forward and Reversed Amplifier3
- Forward Load

As mentioned before, the LLRF handles the interlocks alarms in order to avoid damage in the accelerator cavities or in the RF chains like arcs, vacuum peaks, reflected power and multipacting. The reflected power signals coming from the *tetrodes protection system* (PSYS) are filtered and then sent to a directional coupler in the front end. One output of the coupler is sent directly to the ADCs of the FPGA, the second output is used as a test point. The safety of the RF module is independent of the LLRF, since the PSYS opens its RF switch when it detects too much reflected power in the amplification stages. Master oscillator signal is sent to a directional coupler and one output is sent to a RF detector to be used by the control system to know if the master oscillator generation is failing.

### Up-conversion front end

The up-conversion consists on converting the DACs outputs of the FPGA board (DC signals) to RF signals (175MHz) using a quadrature IQ modulator. The inputs of the modulator are the MO signal and the IQ outputs of the amplitude and phase control loops.

**Local timing system: VCXO PLL**

The local timing system is based on a commercial PLL board from Texas Instruments (CDC7005-EVM) with a 100MHz VCXO and a differential to low voltage TTL<sup>5</sup> (LVTTTL) conversion board developed by [120].

The PLL board has five differential outputs, whose frequency can be independently programmable through a serial peripheral interface (SPI). The FPGA board programs the PLL to be locked with the required external reference signal. It also monitors the status of the PLL giving the following information by means of the LLRF control system interface:

- PLL powered
- Presence of external reference signal
- PLL locked
- SPI cabled disconnected

One of the outputs of the PLL board is programmed to provide a 100MHz clock for the FPGA boards. This clock should be perfectly synchronized (phase locked) with the MO signal in order to perform an accurate sampling of the RF signals. To ensure this synchronization an external signal is sent to each LLRF front end. Ideally, this signal should be a 10MHz Low Voltage Complementary Metal-Oxide-Semiconductor (LVCMOS) signal or compatible provided by the Timing System (TS).

**Pin diode switch**

Two pin diode switches, one per cavity, are placed between the output of the up conversion modulator (RF Drive) and the input of the first amplifier of the RF chain. In case one of the fast interlocks goes to a non safety state, the FPGA board sends a control signal to open the pin switch.

**6.3.1.2 cPCI chassis**

The cPCI chassis allocates the CPU, the FPGA boards (VHS-ADAC from Lyrtech) and the general purpose input/output (GPIO) patch panels. All these units compose the second module of the LLRF and as mentioned before, there are one cPCI chassis per two RF chains.

The chosen cPCI chassis model belongs to the series cPCI-6400 from Adlink, with 5 slots for 6U cPCIs and redundant power supplies

**CPU**

The format of the CPU is 6U cPCI and it works under Windows operating system. It is used to send/receive the configuration commands to/from the FPGA board in order to define the operation mode of the system and it also retrieves the diagnostics signals.

---

<sup>5</sup>Transistor-transistor logic (TTL) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called transistor-transistor logic because both the logic gating function (e.g., AND) and the amplifying function are performed by transistors.

The chosen CPU belongs to the cPCI-6965 Series from Adlink, with low power Intel Core2 Duo 2.2GHz.

#### **FPGA boards (Lyrtech VHS-ADAC)**

The core of the LLRF control loops is a commercial FPGA board with cPCI format from Lyrtech. The main hardware components of this board are:

- FPGA Virtex-4
- 8 ADCs 14 bits resolution, maximum working speed 125MHz
- 8 DACs 14 bits resolution, maximum working speed 400MHz
- RAM memory: 128Mbytes
- GPIO (general purpose input/output) connector of 32 bits
- Internal and external clock source
- External trigger for acquisitions
- Several communications ports

These features correspond to the Loops board. This board receives the loop RF signals (cavity voltage, forward power of the cavity, master oscillator, etc) and it provides the control outputs for the amplitude, phase and tuning loops. An additional VHS-ADC board (Diagnostics board) with 16 ADCs and no DACs is added to the system to measure the RF diagnostics signals.

#### **GPIO patch panel**

Each FPGA board has a GPIO Bus of 32 pins to receive/send signals from/to other systems of the RF plant (PLL, MPS, vacuum, etc). A printed circuit board (PCB) has been designed to distribute all these signals between the different systems.

## 6.4 LLRF control system development

### 6.4.1 Introduction

Considering the LLRF system functionalities shown earlier and the requirements outlined in [5.6.2](#), [5.7.1](#) and [5.8.2](#), the LLRF control system has unique features and an extraordinary responsibility for the overall operation of the accelerator.

As mentioned before, the main element of the LIPAc LLRF control system is a high performance and commercial Lyrtech FPGA VHS-ADC board, with its application programming interface (API) and its low level configuration, that is installed in the cPCI bus of a Windows host computer. The main issue of the LLRF control system is to communicate this Lyrtech board with the EPICS Channel Access and to make all its functionalities controllable and understandable from the EPICS environment.

The LLRF control system has significant differences with the most general developed model used for the local control systems showed in previous sections, i.e., section [5.7](#) or section [5.8](#), accordingly, it can be considered as an exotic solution within this context. Thus, the main property of this control system is the development of an EPICS device driver on the host computer in order to allow the understanding of the card with the upper layers of the control system. Furthermore, it is necessary that the rest of the LIPAc control system, with Linux-based computers, be able at all times to know the status of the LLRF. This is one of the fundamental requirements of any distributed and multilayer control system, see section [3.2](#).

Although the development of the control for the Lyrtech board is considered exotic and have some added difficulties, the choice of that specific FPGA model follows certain technical requirements which are essential for the LLRF system performance. Virtex-4 FPGA allows to fulfill highest processing needs, that is, if an interlock happens, FPGA card is able to make an emergency halt in *less than 10 micro seconds* and to stop sending RF power to the cavities. It provides a very good logic, with one of the highest performance and density, and the memory capacity allows to make accuracy fast data logging. This FPGA board consumes only half the power needed by other FPGA families. As mentioned before, there are two Lyrtech FPGA cards per RF module working in parallel, see Fig. [6.3](#), one is called Loops and the other is known as Diagnostics. One is in charge of the amplitude, phase and tuning loops (Loops board), the other one is in charge of the fast interlocks management and ancillary diagnostics (Diagnostics board).

Some examples of RF systems with EPICS can be found in [\[126\]](#), [\[122\]](#), [\[123\]](#). A solution based on a digital LLRF with a similar board using EPICS with a JAVA IOC can be found in [\[127\]](#) and in [\[128\]](#) for the control of a beam position monitor. Another similar solution can be examined in [\[129\]](#). A quite similar development based LLRF based on Virtex II and EPICS is explained in [\[123\]](#). The work presented here has significantly more functionalities than [\[123\]](#), such as DACs and ADCs gain, system tuning, clock, VCXO programming or fast data logger, see section [6.4.4](#). In addition, there is a fundamental difference between the present work and those exposed above, namely, what is presented to the final user corresponds with an interface where all internal processes related to control and monitoring are transparent.

In conclusion, main contribution of this section is the development of the LLRF control system based on a device driver, see section [4.2.5.4](#), which is able to manage different



applications related to control and monitor processes. Mainly, this device driver is in charge of making the system understand the parameters set by the operators in order to control the RF system and interact with other subsystems that require it. This communication is possible all along the control sites, both locally and remotely. Communication from the board to control system and viceversa is carried out across the architecture shown in the following section.

### 6.4.2 LLRF control system architecture

The utilized architecture, shown in Fig. 6.4, .

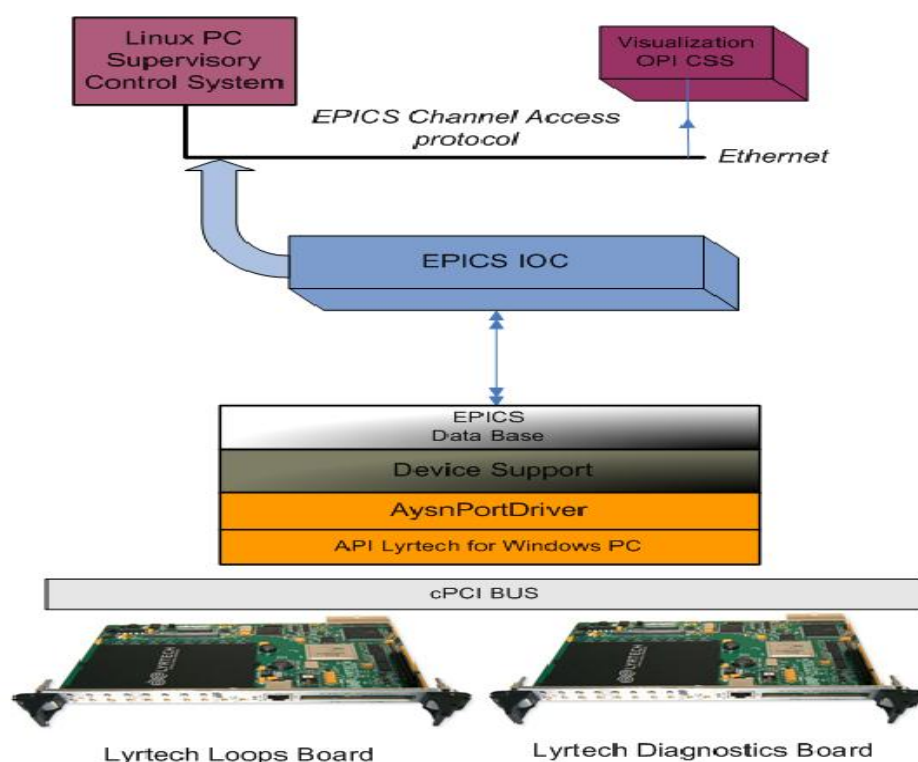


Figure 6.4: LLRF control architecture

This solution consists of the following software components (see section 4.2.5 for specific information of the EPICS components):

- Supervision OPI CSS: Control System Studio (CSS) is a combined effort of several parties, including DESY (Hamburg, Germany) and SNS (Oak Ridge, TN). It provides a collection of control system tools in a common environment, based on Eclipse. The LLRF control system Graphical User Interface (GUI) has been developed entirely using this collection of tools. A complete picture of the GUI main screen can be seen in Fig. 6.5. To insure a consistent look and feel between the panels developed, basic rules have been followed. This aspect must be taken in consideration because GUI panels are the most important way to interact with the different subsystems. A uniform way to

represent information is very important and to avoid overloaded interfaces. The more intuitive the user interface, the more efficient it is. The operator and the machine engineer can easily tune the system, control the parameters and program Lyrtech boards through the set of designed pages. Following the EPICS philosophy, the whole logic involved has not been implemented at the client level (CSS, but rather on the IOC), thus they are available from anywhere in the control system using any EPICS client.

- LAN: Local Area Network. This is the computer network which allows the communication between IOCs and Operator Interfaces (OPIs). EPICS provides a software component, Channel Access, which provides network transparent communication between Channel Access clients (e.g. Operator Interface, OPIs) and an arbitrary number of Channel Access servers (e.g. IOCs).
- EPICS IOC (Input/Output Controller): The IOC is any computer that supports the EPICS run-time components, including the database, and its access routines, device drivers, record types for various input and output and scanning and monitoring functionality. Since the host computer system Lyrtech card is based on Windows, the EPICS IOC runs on a Windows host, LLRF control system running screen IOC can be seen in Fig. 7.3, where it is precisely described. This EPICS IOC starts by loading the binary software image and then a database definition file containing a description of all the data records and enumerated types used in the in-memory database. The `st.cmd` file is short and simple, it uses macros for PVs names that allows the system to make fast changes to the whole set of PVs names. During initialization, the driver detects the boards assigning them a handle that is its main identifier, a `.bit` file is also loaded into the boards memory, which has been specifically written for the features of this system.
- EPICS Database: The EPICS database is a basic element in an IOC. The database is a collection of records of various types. A record is an object with:
  - A unique name
  - A behavior defined by its record type (class)
  - Controllable properties (fields)
  - Optional associated hardware I/O (device and driver support)
  - Links to other records.
- Device Support: it can be defined as an interface between records and hardware. A device support routine has knowledge of the record definition. It also knows how to talk to the hardware directly or how to call a driver which interfaces to the hardware. Thus, device support routines are the interface between hardware specific records in a database record and device drivers or the hardware itself.
- AsynPortDriver: It is the name of the original *asyn* package. It is written in C and provides the functions needed to write asyn servers (called asyn port drivers) and asyn clients (such as EPICS device support). It provides `asynManager`, which is the core of *asyn*, as well as a set of specific interfaces (`asynInt32`, `asynOctet`, `asynFloat64`, etc.). `AsynPortDriver` is a C++ class that is intended to make it much easier to write

asyn port drivers. It takes care of most of the details of writing a port driver. It has a parameter library, and a set of base class methods that can be used in many cases. AsynPortDriver simply calls the original asynDriver functions, which are then more or less hidden from the derived classes that are based on asynPortDriver [14]. Asyn provides standard facilities for debug tracing. Just adding one line to the driver to use this feature. Then, when the user enables *AsynTraceloDriver* at the EPICS shell for the driver (*asynSetTraceMask(myDriver, 0, 9)*) this turns on debugging messages from the driver. Those messages have useful time stamps, and they can be routed to a file, not just to standard output (stdout) [14]. In every record, the DTYP (device type) field determines which device type to use, in this case, the DTYP corresponds with the asynPortDriver [14] functions (*writeInt32*, *writeFloat64* ...). From the record support level, the control goes to record device support which calls asynPortDriver. This device support solution increases the modularity and makes not necessary to learn a new record type for each type of device.

- API Lyrtech: A software provided by the FPGA manufacturer used to communicate with the boards.

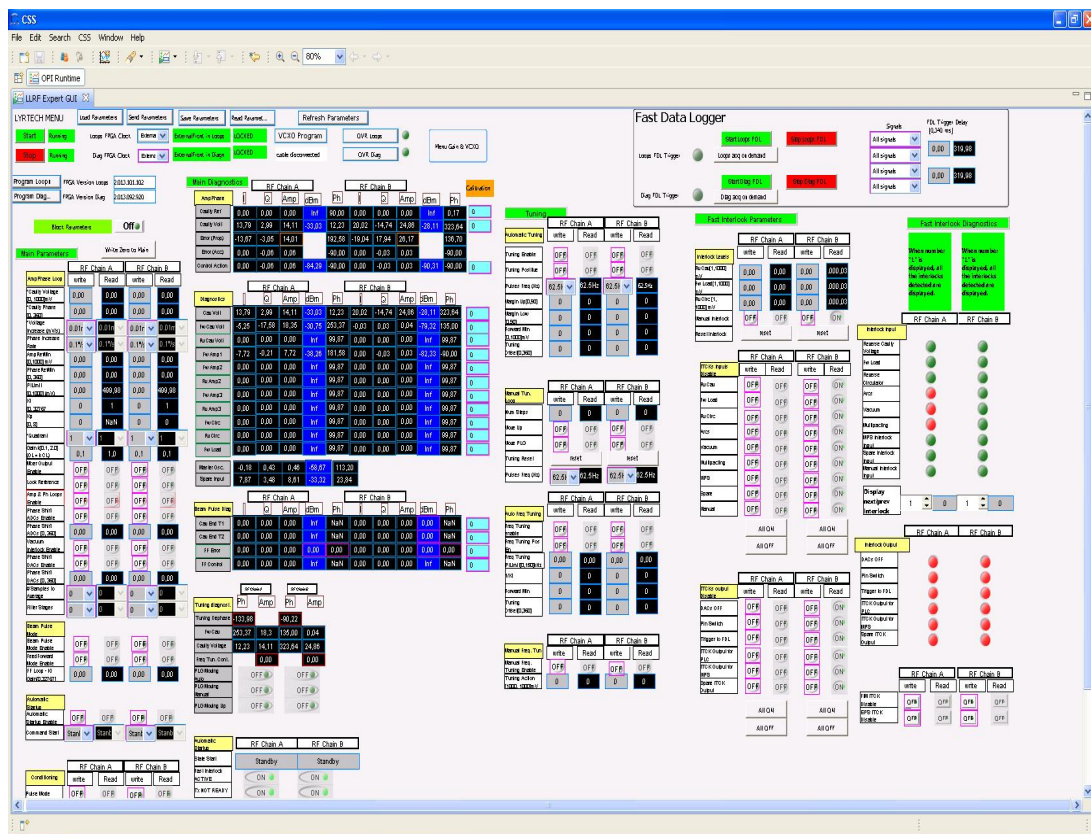


Figure 6.5: LLRF GUI main screen

The above architecture is module-based and has the basic components of a system running EPICS, see section 4.2, as shown in Fig. 6.6. At the client level, CSS is used as OPI

software that allows PVs to be accessed and modified from the network, using the second layer, the Channel Access, that is the communication protocol used by EPICS to transfer information through the network. The next layer is the record support one, where the IOC and the database are located; here, the software which implements PVs for the use with Channel Access is settled. This is the heart of the architecture and permits the communication between records in the database and the driver. The fourth level corresponds with the equipment level, FPGA boards.

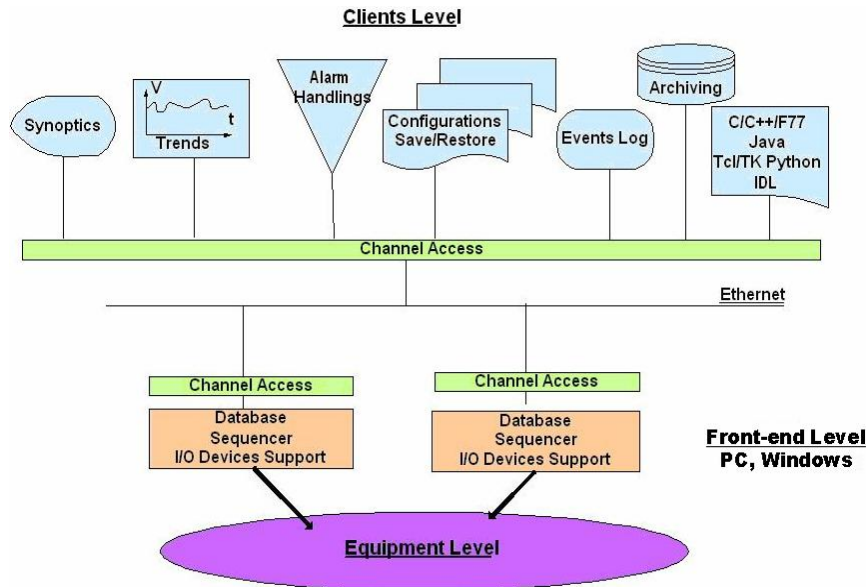


Figure 6.6: Equivalent module-based architecture

The performance of this architecture is tested in section 7.2.1.1. The specific software components used for the developed solution are: EPICS Base 3.14.11, Visual Studio 2008 C++ Express Edition, asyn4-13-1, the specific (API) for this Lyrtech board and Control System Studio (CSS 3.0.2) [130].

### 6.4.3 Control system operation

The standard procedure to operate Lyrtech VHS-ADC/DACs boards is using a commercial software tool included in the purchase. This tool communicates directly with the VHS-ADC/DACs, it must run on the cPCI CPU board of the cPCI chassis that contains the platform. Through this utility, operator can control the FPGA clock and the trigger settings, FPGA designs, the four custom registers, the input/output gains of all the VHS-ADC/DACs and a few more functionalities but all writings and reading must be done using hexadecimal language with the corresponding limitation that it implies. If the program detects the proper modules within FPGA designs, operator can control data recording, as well as data playback. The solution developed in this work is an extension and an improvement of this utility. Moreover, this development offers new extra functionalities and the possibility to control and modify parameters that are not accessible from the traditional utility. In addition, the boards

can be controlled both locally and remotely, that provides the system the ability to work on a distributed control system. Finally, The operator does not need to speak the *same language* as the card and do not need to understand hexadecimal addresses of the registers, write/read operations are now transparent for the user.

In order to achieve the general control system operation and the below functionalities, the device driver code length developed has  $\approx 10000$  lines and it is growing thanks to the addition of new features and improvements.

#### 6.4.3.1 Parameters to/from FPGA

Each device driver is used to control the LLRF system of two RF chains. In order to do so, the operator sets some working parameters. All these settings are gathered in different groups in the GUI and all these sets of parameters are normally separated between chain A and chain B:

- Amplitude and phase loop parameters
- General configuration parameters
- Tuning loop
- Manual tuning
- Conditioning
- Interlocks parameters and diagnostics
- Diagnostics parameters
- Fast data logger parameters

As mentioned, the device driver is based on the use of certain functions such as *read/write* registers in the Lyrtech board. The general way to write and read parameters is as follows: when the operator writes a new parameter in the GUI, this parameter is sent to the FPGA through Register 0. The device driver applies the right transformation to the parameter value. FPGA registers allow to the user sending 32 bits words to the board. The 16 MSBs are employed as the address of the word, while the 16 LSBs are used to send the data or value of the parameter. The MSB bit is set to 1 when sending a parameter to cavity A and set to 0 when sending a parameter to cavity B. Both cavities have the same number of parameters, but their values could be different. Besides, every parameter is sent twice in two different addresses in order to avoid communications problems. In case the data sent by the two addresses are not coincident, a diagnostics error bit is asserted and stored in another register. Bits 30 to 17 are identical in these two addresses, and bit 16 is set to 0 for the first address and set to 1 for the second address. Some examples of this operation are shown in Fig. 6.7.

After writing a new parameter, the driver reads instantly the new information from the FPGA once it has been written. To do so, the driver writes the parameter address in Register 1 and then it reads back the value of Register 1.

On the other hand, all the parameters are not taken into account by the FPGA until the word 1 (MSB=0), for chain A, or word 2147483649 (MSB=1), for chain B, be sent to the Register 3. This is done every time a new parameter is set and after that, Register 3 is set to zero again.

	GUI Value	Value to be sent to FPGA	Cavity Selection (bit 31)	ADDRESS (From bit 30 to bit 17)				Address selection	DATA (from bit 15 to bit 0)							
Bit Position			31	32	...	18	17	16	15	14	13	...	2	1	0	
Kp A (1 <sup>st</sup> address)	1	1	0	0	0	0	0	0	0	0	0	...	0	0	1	
Kp A (2 <sup>nd</sup> Address)		65537	0	0	0	0	0	1	0	0	0	...	0	0	1	
Ki A (1 <sup>st</sup> Address)	1	131073	0	0	0	0	1	0	0	0	0	...	0	0	1	
Ki A (2 <sup>nd</sup> Address)		196609	0	0	0	0	1	1	0	0	0	...	0	0	1	
IRef A (1 <sup>st</sup> Address)	100	527565	0	0	1	0	0	0	0	0	0	...	1	0	1	
IRef A(2 <sup>nd</sup> Address)	100	593101	0	0	1	0	0	1				...				
Kp B (1 <sup>st</sup> address)	1	2147483649	1	0	0	0	0	0	0	0	0	...	0	0	1	
Kp B (2 <sup>nd</sup> Address)		2147549185	1	0	0	0	0	1	0	0	0	...	0	0	1	
Ki B (1 <sup>st</sup> Address)	1	2147614721	1	0	0	0	1	0	0	0	0	...	0	0	1	
Ki B (2 <sup>nd</sup> Address)		2147680257	1	0	0	0	1	1	0	0	0	...	0	0	1	
IRef B (1 <sup>st</sup> Address)	100	2148011213	1	0	1	0	0	0	0	0	0	...	1	0	1	
IRef B (2 <sup>nd</sup> Address)		2148076749	1	0	1	0	0	1	1			...				

Figure 6.7: Example parameter values and addresses to be written in Register 0

### 6.4.3.2 Device driver parameters transformation

The digital IQ demodulation, which is out of the framework of this thesis [120], is carried out at FPGA level. For doing so, the RF inputs are under-sampled and digitally demodulated. Since the CPU is used to send-read configuration commands to-from the FPGA board, some of the values displayed in the GUI need to be transformed by the device driver. These special parameters are for example: *Cavity Voltage*, *Cavity Phase*, IQ components and some diagnostics. The challenge of these transformations is to make the board understand values that the operator can easily manage and to get values from the FPGA in order to be understood both by the EPICS Channel Access and the operator. Hence, the first step to control amplitude and phase components of the Cavity Voltage, is to transform the Cavity Voltage set points introduced by the operator through the GUI from polar coordinates (amplitude and phase) to rectangular coordinates (I and Q). The device support performs these operations using the formulas shown in Fig. 6.8.

GUI parameter	FPGA parameter	Relation between GUI and FPGA parameter
Cavity Voltage and Phase cavity voltage	IRef & QRef	$\text{IRef} = \text{Cavity Voltage} \cdot \cos(\text{Cavity Phase})$ $\text{QRef} = \text{Cavity Voltage} \cdot \sin(\text{Cavity Phase})$ $\text{Cavity Ref Amp} = \sqrt{\text{IRef}^2 + \text{QRef}^2}$ $\text{Cavity Ref Phase} = \text{atan}(\text{Q} / \text{I})$ $\text{Amplitude} = \sqrt{\text{I}^2 + \text{Q}^2}$ $\text{Phase} = \text{atan}\left(\frac{\text{Q}}{\text{I}}\right)$

Figure 6.8: Relation between FPGA-GUI GUI-FPGA parameters

### 6.4.3.3 Diagnostics implementation

A very important goal of the RF power system design is the strong availability and maintainability requirements for IFMIF accelerator. The high number of components of the entire system sheds a not negligible fault probability, even if each element has a high level of reliability.

When a fault occurs in a conventional RF facility, the accelerator must be stopped, the problem should be fixed and defective element removed. All of this can take a significant time, moreover sometimes it is necessary to remove equipments that have not failed but impede the access to the failed device. The diagnostics are used to continuously monitor the status of the RF power system in order to avoid failures before they happen instead of merely wait to detect them. Stringent reliability and maintainability goals are set for the RF power system.

Consequently, dozens of diagnoses have been implemented in the LLRF control system. Expert GUI with several diagnoses can be seen in Fig. 6.9.

In general, all system diagnostics readings are held every second. There is a function in the driver, called *ReadStatus*, issuing this term, it writes the address of the parameters associated with the diagnosis in the appropriated register and reads back its value.

The next piece of code shows how some of the diagnoses have been implemented in the EPICS record database:

```
record(ai,(P)(R)CAVA : IrvCircRdbk) {
  field(DTYP, asynFloat64)
  field(INP, @asyn$(PORT),$(ADDR),$(TIMEOUT))irwcirc)
  field(HIHI,"1000")
  field(HHSV,"MAJOR")
  field(HIGH,"900")
```



Main Diagnostics										
AmpPhase	RF Chain A					RF Chain B				
	I	Q	Amp	dBm	Ph	I	Q	Amp	dBm	Ph
Cavity Ref	0,00	0,00	0,00	Inf	45,00	0,00	0,00	0,00	Inf	45,00
Cavity Volt	0,00	0,00	0,00	Inf	45,00	0,00	0,00	0,00	Inf	45,00
Error (Prop)	0,00	0,00	0,00		45,00	0,00	0,00	0,00		45,00
Error (Acc)	0,00	0,00	0,00		45,00	0,00	0,00	0,00		45,00
Control Action	0,00	0,00	0,00	Inf	45,00	0,00	0,00	0,00	Inf	45,00

Diagnostics	RF Chain A					RF Chain B				
	I	Q	Amp	dBm	Ph	I	Q	Amp	dBm	Ph
Cav Volt	0,00	0,00	0,00	Inf	45,00	0,00	0,00	0,00	Inf	45,00
Fw Cav Volt	0,00	0,00	0,00	Inf	45,00	0,00	0,00	0,00	Inf	45,00
Rv Cav Volt	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Fw Amp1	0,00	0,00	0,00	Inf	45,00	0,00	0,00	0,00	Inf	45,00
Fw Amp2	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Rv Amp2	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Fw Amp3	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Rv Amp3	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Fw Circ	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Rv Circ	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Fw Load	0,00	0,00	0,00	Inf	99,87	0,00	0,00	0,00	Inf	99,87
Master Osc.	0,00	0,00	0,00	Inf	45,00					
Spare Input	0,00	0,00	0,00	Inf	45,00					

Figure 6.9: Diagnostics of LLRF control system

```

field(HSV,"MINOR")
field(PREC,2)
field(SCAN,I/OIntr") }

```

There are two relevant things to emphasize in the above piece of EPICS database code:

- Alarm system. Fields named HIHI, HHSV, HIGH and HSV belong to the alarm system. These record fields have correspondence with the GUI through the database. Limits which activate the alarms are taken from PV. One of the properties that can be activated if a value is exceeded is *border alarm sensitive*. If yes, border color and style changes to alarm border style and color when PV is in alarm and so on with the rest of limits and colors defined.
- Scan. Scanning determines when a record is processed. A record is processed when it processes its data and performs any actions related to that data. For example, when an output record is processed, it fetches the value which it is to output, converts the value, and then writes that value to the specified location. Each record must specify the scanning method that determines when it is processed. There are three scanning methods for database records: periodic, event, and passive. In this, even scanning with I/O interrupt events is used. Scanning on I/O interrupt causes a record to be processed when the I/O card from which it gets its value, generates an interrupt. For example, if an analog input record gets its value from any change in the beamline configuration and it specifies I/O interrupt as its scanning routine, then the record is processed each time the card generates an interrupt (not all types of I/O cards can generate interrupts). In order for a record to scan on I/O interrupts, its SCAN field must specify I/O Intr. In addition of this scanning type there is a periodic scanning set on time intervals of



one second and there is also a *refresh parameters* button ready to be used at any time. The performance of the scanning is shown in 7.2.1.1.

#### 6.4.3.4 Synchronous and asynchronous device driver

Because `asynPortDriver` is used, almost all of the details of synchronous versus asynchronous are taken care of. Therefore, the choice of using a simple synchronous device is not considered. The only thing needed to do to change from synchronous to asynchronous is set the bit mask for *AsynCanblock* in the call to the `asynPortDriver` constructor in the driver. Then, the code looks like this: *AsynCanblock=0*, *AsynMultidevice=1*, *autoConnect=1*.

That means that a synchronous driver is created as well, i.e., one that is assumed to execute quickly (e.g. under 1 ms, so it does not slow down EPICS record processing). If the device is *slow* and to create an asynchronous driver is needed, then changing this to: *AsynCanblock=1*, *AsynMultidevice=1*, *autoConnect=1* is enough.

The difference is all handled by `asynManager` and the standard asyn device support.

If the *AsynCanblock* bit is not set, then device support directly calls the driver's *writeInt32*, *readInt32*, etc. functions when the record processes from whatever thread is processing the record i.e., EPICS periodic scan tasks, Channel Access server tasks, etc. This should only be done if the device is fast, see Fig. 6.10.

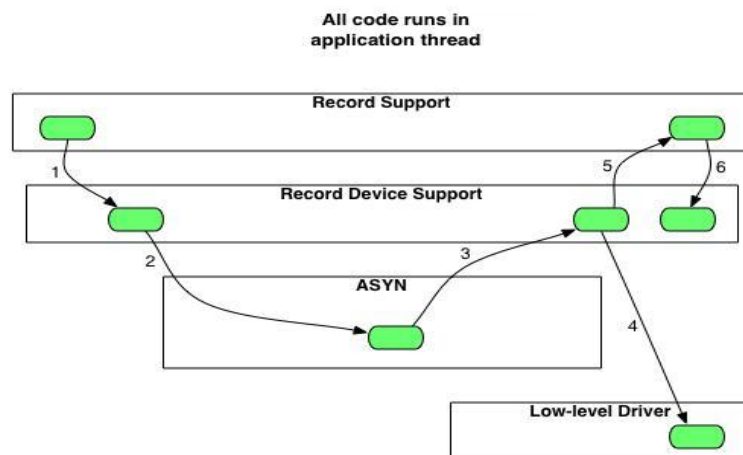


Figure 6.10: Device support communicating with an synchronous device [14].

If the *AsynCanblock* flag is set, then *asynManager* function creates a separate port thread for the driver. When device support wants to talk to the driver it queues a request to communicate with it, and when the driver is not busy, device support calls the driver from that separate port thread. The driver is allowed to be slow in this case, because it does not block record processing, see Fig. 6.11.

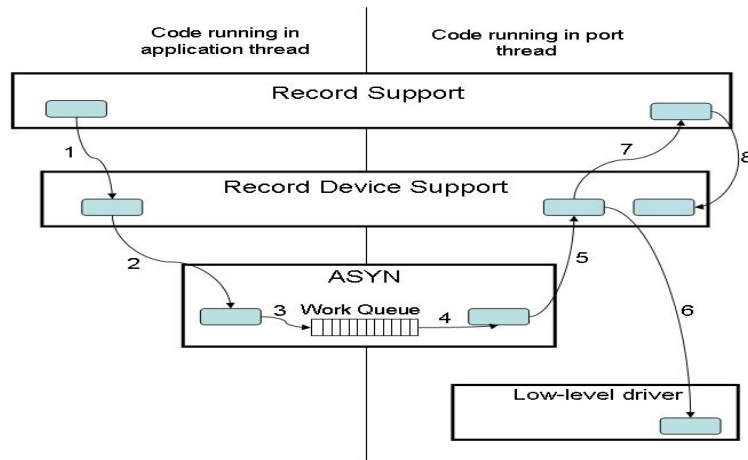


Figure 6.11: Device support communicating with an asynchronous device [14].

#### 6.4.4 Device driver functionalities

The device driver has several functionalities and hundreds of signals to manage. All features are developed in order to match control requirements, they are necessary for the proper functioning of the subsystems within the LIPAc purposes.

##### 6.4.4.1 Gain

The applicable gain range of the VHS-ADC Virtex-4 ADC and DAC channels is 0 to 15 (i.e. 4-bit gain values). The device driver allows the user modifying the values of these gains to the required set point. The performance of this solution is shown in 7.2.1.3.

##### 6.4.4.2 Clock

All the operations carried out by the Lyrtech board should be synchronized with a clock. The source of this clock can be internal or external.

The device driver allows the user to choose any of these clock configuration:

- External source
- Fixed on board clock (105MHz)
- FPDP Receive Clock
- RapidCHANNEL Receive Clock
- FPGA Generated
- Fixed Divided by Two

For the LLRF system internal tests, the clock option is always used: *external source from front panel*. The Lyrtech board is configured by default to work with this clock source.

6.4.4.3 Voltage Controlled Crystal Oscillator(VCXO)

The function of the VCXO, Fig. 6.12, is to synchronize Lyrtech card clock with master oscillator signal in order to properly perform the IQ demodulation of RF signals.

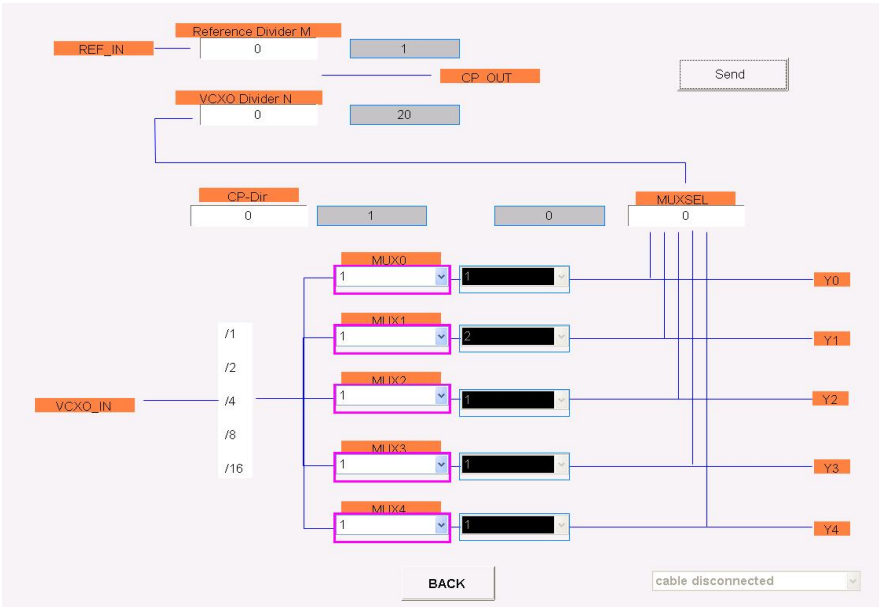


Figure 6.12: VCXO main control screen

Without the VCXO, the phase of the RF signals could not be read. Main properties of this functionality are:

- Synchronizes frequencies up to 800 MHz
- Each output frequency is selectable by x1, /2, /4, /8, /16
- All outputs are synchronized

Table 6.1: Relation between bits and displayed messages in VCXO control status

VCXO				
Power (50)	Ref (51)	Locked (52)	Cable (53)	message to display
x	x	x	1	VCXO cable disconnected
1	0	0	0	VCXO Powered
1	1	0	0	VCXO Reference
1	1	1	0	VCXO Locked
Any other combination of bits				Error

In order to check if the VCXO has been well programmed, the device driver read the status of the four diagnostic signals with addresses 50 to 53 as shown in table 6.1. The way

to read these bits is the same employed to read any diagnostics signals, i.e., to write the address of the corresponding signal in register 2, and to read back the register value. The FPGA understands the bit combination but the user is only aware of the messages to display, the correspondence between bits and messages is done at device driver level.

#### 6.4.4.4 Control of the tuning loop

Once the accelerator operation is started, the shape of the cavity, and consequently its resonance frequency, can vary greatly due to certain physical changes caused by the beam injection, thus, it is necessary to tune cavity to reach again to the proper resonance frequency. The tuning loop of the cavities measures the phase difference between the cavity voltage and the forward cavity voltage. In the MEBT case, when the phase difference is out of a certain margins, the board sends a train of pulses (LVTTL) to move a stepper motor changing the geometry of the cavity and its resonance frequency. The frequency of the pulses can be varied by the operator (from 50Hz to 2kHz) to adjust the speed of this loop. A second LVTTL signal is also sent to the stepper motor to indicate the direction of the movement, inwards or outwards the cavity body, more details of the LLRF and the MEBT interface are given in section 6.4.5 and the performance of the development for the control of the plunger through the LLRF control system GUI is detailed in 7.2.1.4.

In section 6.4.5 the interface between SRF Linac and LLRF system is explained, detailing the control for the tuning of the SRF Linac cavities. To achieve the control of this loop, a group of related parameters has been implemented in the device driver. SRF Linac subsystem moves a tuner using the data provide by the LLRF control system, in order to adjust the resonance frequency of the cavity minimizing the reflected power of the cavity.

Regarding to RFQ, to guarantee the tuning and a correct distribution of the power in the RFQ cavity, the LLRF will measure the voltage of the cavity in four pick-ups, see section 6.4.5. One of these signals, the master one, will be used for the tuning loop. The LLRF will compute the phase difference between the master cavity voltage and the forward master drive and it will send this information to the Channel Access. The RFQ cooling system will adjust the general temperature of the cavity depending on the value of the phase difference to keep the resonance frequency of the cavity constant.

The LLRF control system also monitors some other signals involved in this loop to know its status and performance, in Fig. 6.13 tuning parameters can be observed in the LLRF control system interface, they are the following:

- Tuning dephase
- Amplitude of the cavity voltage and forward cavity voltage
- Status of tuning loop (on/off)
- Warning message when the cavity is too out of tune (tuning diphas bigger than 180 degrees)

The screenshot displays the LLRF GUI with two main sections: 'Motor Tun. Loop' and 'Manual Tun. Loop'. Each section has controls for 'RF Chain A' and 'RF Chain B', including 'write' and 'Read' buttons. The 'Motor Tun. Loop' section includes parameters like 'Tuning Enable', 'Tuning Positive', 'Pulses Freq (Hz)', 'Margin Up', 'Margin Low', 'Forward Min', and 'Tuning Offset'. The 'Manual Tun. Loop' section includes 'Num Steps', 'Move Up', 'Move PLG', 'Tuning Reset', and 'Pulses Freq (Hz)'. In the image, several 'OFF' buttons and '62.5Hz' dropdown menus are highlighted with pink boxes.

	RF Chain A		RF Chain B	
	write	Read	write	Read
<b>Motor Tun. Loop</b>				
Tuning Enable	OFF	OFF	OFF	OFF
Tuning Positive	OFF	OFF	OFF	OFF
Pulses Freq (Hz)	62.5Hz	62.5Hz	62.5Hz	62.5Hz
Margin Up[0,90]	0	0	0	0
Margin Low [0,90]	0	0	0	0
Forward Min [0,1000]mV	0	0	0	0
Tuning Offset[0,360]	0	0	0	0
<b>Manual Tun. Loop</b>				
Num Steps	0	0	0	0
Move Up	OFF	OFF	OFF	OFF
Move PLG	OFF	OFF	OFF	OFF
Tuning Reset	reset		reset	
Pulses Freq (Hz)	62.5Hz	62.5Hz	62.5Hz	62.5Hz

Figure 6.13: Tuning parameters on the LLRF GUI

#### 6.4.4.5 Control of the automated conditioning

The conditioning process seeks to ensure the operation of cavities with large electric fields in the interior, which is necessary for removing particles adhering to the walls of the cavities so as to maintain high vacuum level. The surface roughness of the cavity is also improved by decreasing the presence of spots that can facilitate electrical arcing in the accelerator operation. This process involves the application of RF energy high power levels and variable work cycles. RF fields induce high voltage potential within the cavities that strip electrons of its metal walls which impact on the opposite walls, releasing the impurities adhered to the cavity and performing a process of surface polishing.

The automated conditioning consists of sending a square RF modulated signal to the cavity. The operator is able to adjust the amplitude and the duty cycle of the pulses. These parameters, amplitude and duty cycle, are increased smoothly with an adjustable slope to avoid sudden increases of vacuum pressure.

The PLC of each RF module has two switches outputs connected to the LLRF GPIO pins. Each switch remains close when the vacuum pressure is below a certain range, one of them gets open at a lower pressure level and the second one gets open at a higher pressure level, but always below the safety vacuum interlock thresholds defined by the operator through the control interface.

To control of cavities conditioning, the operator can also set the maximum power level. The LLRF then starts increasing the power at a speed defined by the operator through the GUI. If the vacuum pressure is below certain limits, the power increase continues (first switch close). In case the vacuum pressure reaches the higher vacuum level (second switch open), it

stops increasing/decreasing the RF power. When the pressure goes down again to the lower level (first switch close), the RF power continues increasing/decreasing. Power corrections are not carried out at device driver level but at a FPGA level.

#### 6.4.4.6 Control of the automated startup

In order to make easier the recovery of the RF plants from an interlock or a shut down, the LLRF has an automated start up mode. The sequence is as follows

- RF presence in the cavity.
- Tuning enabled: Tuning of the cavity at low power.
- Amplitude and phase loops enabled at low power.
- Smooth increase of power until the set point is reached.
- RF ready for operation with beam.

When automatic startup is enabled, the LLRF follows a sequence of tasks before sending to the operator the message: *Ready for operation with beam*. In case one of the stages could not be accomplished, the GUI shows an error message.

#### 6.4.4.7 Fast data logger (FDL)

Lyrtech Boards, Loops and Diagnostics, have a 128 RAM which is storing data continuously. After an interlock happens, the LLRF sends a trigger to stop the acquisition of signals and all the data stored in the RAM is transferred to a binary file. All the parameters stored in the registers for the slow diagnostics are as well stored in this circular buffer at 100 MHz speed. The diagnostic signals are multiplexed and sent to the memory through a bus of 16 bits. The information is retrieved and sent to the host PC for post mortem analysis when an interlock occurs or under an operator request. With these specifications, the retrieved information corresponds to a maximum of 330ms of operation.

All FDL parameters can be configured through the GUI. The operator can select the signals that will be stored if an interlock happens. The operator can even modify the size of storage by modifying the acquisition time.

#### 6.4.4.8 Autosave module

All the I&Q components of the RF signals and other signals involved in the digital signal processing of the FPGA boards are stored in registers of the board to be accessed by the local control system. Data are monitored and stored at 1Hz rate to have an historical archiving of the system performance, these diagnostics are stored using autosave module.

Autosave automatically saves the values of EPICS process variables (PVs) to files on a server, and restores those values when the IOC is rebooted. Autosave is a two-part operation:

run-time save, and boot-time restore. The run-time part (the save-restore task or thread) is started by commands in the IOC startup file, and persists while the IOC is running. Its primary job is to save PV values to files on a server, but it also supports manual restore and other management operations. The boot-time part (`dbrestore.c`) is invoked during `iocInit`, via an EPICS *initHook*. It restores PV values from files written by the run-time part, and does not persist after `iocInit()` returns [131].

#### 6.4.4.9 Control and configuration of the interlocks parameters

As explained before, an interlock system is integrated in the LLRF to handle any alarm that could represent damage for the accelerator cavities and/or the RF chains. If an interlock detection happens, LLRF system immediately stop sending RF power to the cavity that has sent the alarm, by means of a pin switch. Besides, LLRF send a hardwired signal to the MPS, then a fast beam inhibition happens. All of these actions are carried out without any EPICS software processing. Nevertheless, the device driver has knowledge of these alarms and transform them into PVs in order to read its status back and to send them to the EPICS Channel Access. In addition to these diagnostics, the operator can configure certain features of the interlock system.

In order to manage the interlock system, several parameters can be accessed and modified through the Fast Interlock Module (FIM) on the LLRF control system interface, see Fig. 6.14. FIM is comprised of two parts, *Fast Interlocks Parameters* which are used to configure the interlock acquisition and *Fast Interlocks Diagnostics* where all the readbacks coming from or sending to the Channel Access are showed. The implementation of the FIM control is developed over the Diagnostics board to ensure there will be no interferences or bugs problems in case Loop board must be replaced or upgraded.

As explained, there are two distinct parts, the configurable part mainly formed by ON/OFF buttons and the one that corresponds to the readings of the interlocks with red/green leds. The optimal operation of the accelerator must be carried out taking into account any type of interlock, but it is possible that during startup or during a specified test, it is required to disable some interlocks, for that purpose, ON/OFF buttons can be used. Disabling an interlock means that if it occurs it will not be taken into account, in fact, the indicator will always remain green. As mentioned before, the list of actions is also configurable using ON/OFF buttons.

The interlocks levels tab, upper left side, basically allows the user to set the maximum reflected power that should be allowed before triggering an interlock. The *manual interlock* has been implemented for testing purposes. When the user enables this button, the system will act as if a real interlock has happened. Reset button is used to come back to a normal state after an interlock alarm is detected and fixed.

The operator can disable/enable any input/output of the interlock signals for testing purposes. In case there is more than one interlock at the same time, the LLRF records the sequence of the interlocks and the GUI displays the time elapsed between the first one and the following ones.

The list of possible actions after an interlock detection is known as *interlocks outputs*. These outputs have associated PVs that activate different leds on the interface once the

FPGA board sends the proper signal indicating if the actions selected by the operator have been achieved.

- DACs OFF: The outputs of the DACs are set to its minimum value
- Pin switch: the LLRF drive stops opening a pin switch controlled by the FPGA.
- Trigger to FDL: Trigger to stop the signal acquisition for post mortem analysis.
- Loops outputs disable: the outputs of the amplitude, phase and tuning loops are disabled.
- Output for PLC: The LLRF system alerts PLC through a LVTTTL signal.
- Output for MPS: The LLRF system alerts MPS through a LVTTTL signal.
- Output for spare interlock.

The interlock module in the device driver is developed using a byte monitor, which is a widget that displays the bits in an integer or long integer value as a set of LEDs. The code created within this byte monitor is as follows:

```
if (function == LYRTECHVHSTimestamp)
stamp = value;
Vhsadac16_WriteFpgaReg(this->current_hADC_D, this->registro2, 99 + value);
diagnostic = Vhsadac16_ReadFpgaReg(this->current_hADC_D, registro2);
setIntegerParam(0, LYRTECHVHSFidTotal, diagnostic);
setIntegerParam(0, LYRTECHVHSTimestamp, 0);
```

To develop the fast interlocks diagnostics using byte monitor provides the control system interface with response times in the milliseconds range. The characterization of this solution is detailed in [7.2.1.2](#).



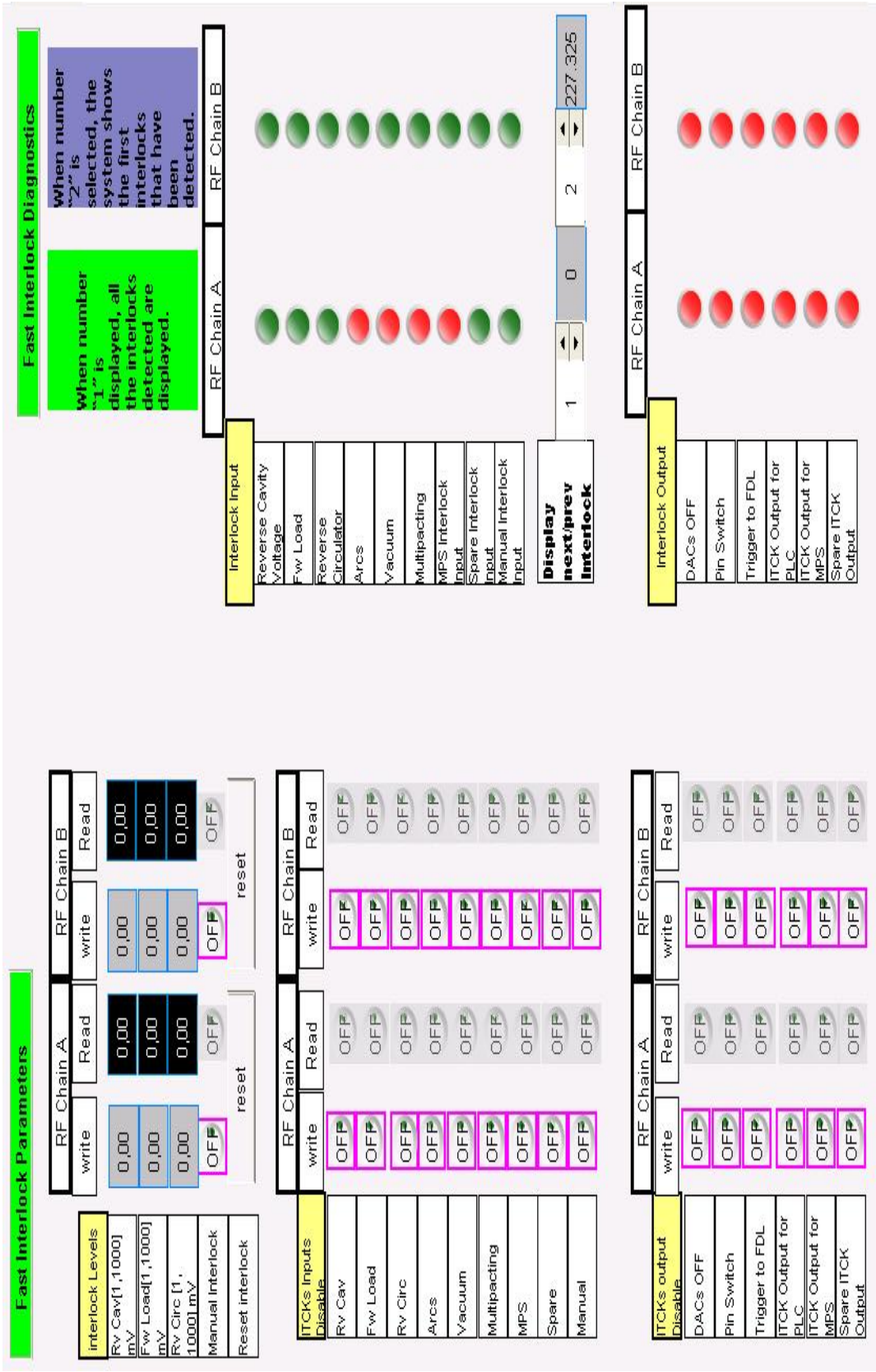


Figure 6.14: Fast Interlock Module

#### 6.4.4.10 Automatic power adjustment

Signals from LLRF have to pass through switchers and couplers devices located inside the main box of the protection system. These devices enable RF path breaking in case of any emergency situation. While in normal operation insertion losses are below 3dB, RF signal coming from the master oscillator with a maximum power level of -3dB should be amplified in the solid state predriver with a gain about 63dB. The LLRF control system has a functionality in which the operator can enter a constant  $k$  of losses that is applied to the entire power readings from the cavity, therefore the operator can add the losses in the readbacks diagnostics for a better understanding of the system behavior.

### 6.4.5 LLRF control system interfaces

As noted before, LLRF system interacts directly with three subsystems: RFQ, MEBT and SRF Linac. Thus, in order to carry out the amplitude and phase loops and the monitoring of the diagnostics and interlocks signals, LLRF control system must be able to interchange PVs in a real-time automatically closed cycle using the EPICS Channel Access. Control interfaces with the mentioned subsystems are detailed in the following sections.

#### 6.4.5.1 LLRF-RFQ interface

As explained in section 5.10, RFQ cavity is powered by 8 RF chains at 200KW. LLRF system carries out the amplitude and phase loop in order to have in the RFQ cavity the desired RF power. For that, forward cavity signals, reverse cavity signals and pick-up<sup>6</sup> RF signals are sent to the LLRF system. After internal loop operations, the output corresponds to the master drive signal that is directly sent to RFQ cavity. Another 7 drives, which should be equivalent in phase and amplitude, are also sent to the other RF chains (slave drives). To guarantee the equivalence between master and slaves signals, slave forward power signals are measured and compared to the master forward signal. LLRF system corrects any deviation between them, compensating non linearity and offsets between the different RF chains. All parameters obtained after these operations are transformed by the LLRF control system into EPICS PVs containing amplitude and phase status, I&Q components of the RF signals, besides the reverse and forward cavity diagnostics.

In order to achieve the tuning in the RFQ cavity, one of these pick-up voltage signals, the master one, is used. LLRF system computes the phase difference between the pick-up cavity master and the forward cavity master, as a result, a parameter called tuning dephase is obtained. The LLRF control system transforms this parameter into a PV and send it to the Channel Access, thus it can be accessed by the RFQ control system. RFQ cooling system adjusts the general temperature of the cavity depending on this tuning dephase PV value, in order to keep the resonance frequency of the cavity constant.

On the other hand, RFQ control system reads the mentioned amplitude and phase status PVs from the Channel Access in order to know the power field distribution in the RFQ

<sup>6</sup>The RF pick-up is an antenna, with optimized length and positioning on the cavity, which consists to measure RF level inside the cavity, without disturbing the field lines

cavity and to guarantee a correct distribution of the power. In case the power in a section of the cavity is higher or lower than the others, the cooling system of the RFQ adjusts the temperature of that section to have a flat field along the body of the cavity, using the information obtained from the Channel Access. Interfaces between LLRF and RFQ are showed in Fig. 6.15.

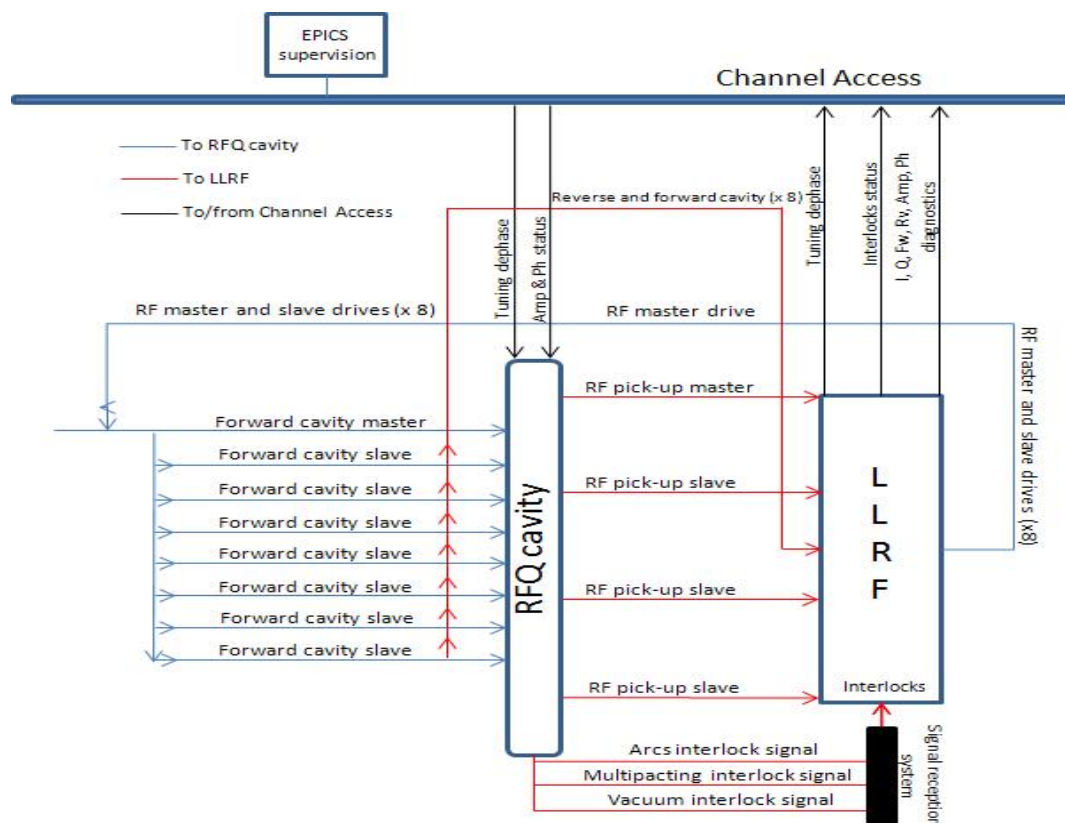


Figure 6.15: Signals interface between RFQ and LLRF

RFQ subsystem also send interlock signals to the LLRF system. Interlock signals are related to arcs detection, vacuum and multipacting. LLRF system manages 8 digital signals for arcs, 8 for vacuum and 8 for multipacting, that is, one signal of each interlock per chain. Every time the LLRF system receives an interlock alarm, the RF power is immediately cut off. Then, LLRF control system control activates two interlock alarm indicators and reports the sequence of actions triggered, see 6.4.4.9 for more details.

#### 6.4.5.2 LLRF-SRF Linac interface

As explained in section 5.10, SRF Linac is powered by 8 RF chains at 105KW. LLRF system carries out the amplitude and phase loop in order to have in the SRF Linac cavities the desired RF power. For that, LLRF system receive the RF level by means of RF pick-ups and executes a loop for each cavity as shown in Fig. 6.16, a measurement of the RF signal is sent to the LLRF system from each SRF Linac cavity. After internal loop operations, the output

corresponds to the RF drive signals that are directly sent to SRF cavities to correct the forward signal. All parameters obtained after these operations are transformed by the LLRF control system into EPICS PVs containing amplitude and phase status, I&Q components of the RF signals, besides the reverse and forward cavity diagnostics.

To achieve the tuning of the SRF Linac HWR cavities, there is a mechanical compression system which uses a deformation tuner for its operation. Tuner moves depending on phase thresholds with respect to nominal HWR cavities phases. Therefore, the tuner needs two parameters to carry out the deformation, namely, *tuner pulse* indicating if the phase excursion is above or below the threshold and *tuner direction* indicating the sign of the phase excursion. Once this threshold is passed, tuning is performed. LLRF control system is in charge of sending these parameters to the EPICS Channel Access in order to be received by the SRF Linac LCS, then the mechanical compression system makes the tuning taking into account this information.

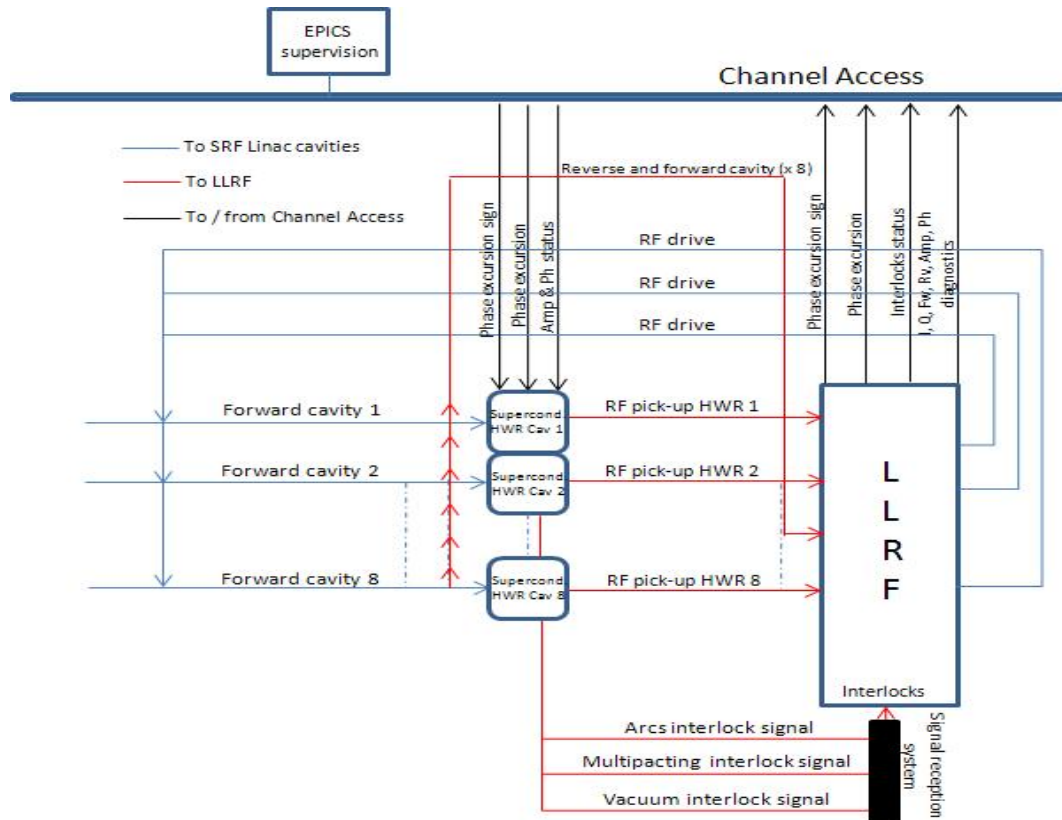


Figure 6.16: Signals interface between SRF Linac and LLRF

SRF Linac subsystem also send the interlocks signals to the LLRF system. Interlock signals are related to arcs detection, vacuum and multipacting. LLRF system manages 8 digital signals for arcs, 8 for vacuum and 8 for multipacting, that is, one signal of each interlock per SRF Linac HWR cavity. Every time the LLRF system receives an interlock alarm, the RF power is immediately cut off. Then, LLRF control system control activates two interlock alarm indicators and reports the sequence of actions triggered, see 6.4.4.9 for

more details.

#### 6.4.5.3 LLRF-MEBT interface

As explained in section 5.10, SRF Linac is powered by 2 RF chains at 16KW. LLRF system carries out the amplitude and phase loop in order to have in the MEBT cavities the desired RF power. For that, LLRF system receive the RF level by means of RF pick-ups and executes a loop for each cavity as shown in Fig. 6.17, a measurement of the RF signal is sent to the LLRF system from each one of the two MEBT cavities. After internal loop operations, the output corresponds to the RF drive signals that are directly sent to the buncher cavities to correct the forward signal. All parameters obtained after these operations are transformed by the LLRF control system into EPICS PVs containing amplitude and phase status, I&Q components of the RF signals, besides the reverse and forward cavity diagnostics.

To achieve the tuning of the MEBT buncher cavities there is movable plunger. A stepper motor would shift the copper movable plunger in order to keeps resonance frequency constant during operation. The stepper motor controller needs therefore some information from the LLRF system which is, one more time, in charge of the amplitude and phase loop and the cavity tuning. First, the motor controller needs a signal to determine the direction of rotation of the motor, which is defined as ON for upward and OFF for downward. Second, the controller needs to know the plunger pulse, the motor performs one step for each rising pulse edge. The number of output pulses determines the angle of rotation, that is, the path to be traveled. And third, the pulse frequency, which determines the rotational speed, that is, the traversal velocity. Unlike the RFQ and the SRF Linac tuning systems that are executed by their LCSs, all these parameters can be defined using the LLRF control interface because in the MEBT case, the LLRF is in charge of moving the plunger and tune the cavity. Tuning and stepper motor parameters are also sent to the EPICS Channel Access.

MEBT subsystem also send the interlocks signals to the LLRF system. Interlock signals are related to arcs detection, vacuum and multipacting. LLRF system manages 2 digital signals for arcs, 2 for vacuum and 2 for multipacting, that is, one signal of each interlock per SRF Linac HWR cavity. Every time the LLRF system receives an interlock alarm, the RF power is immediately cut off. Then, LLRF control system control activates two interlock alarm indicators and reports the sequence of actions triggered, see 6.4.4.9 for more details.

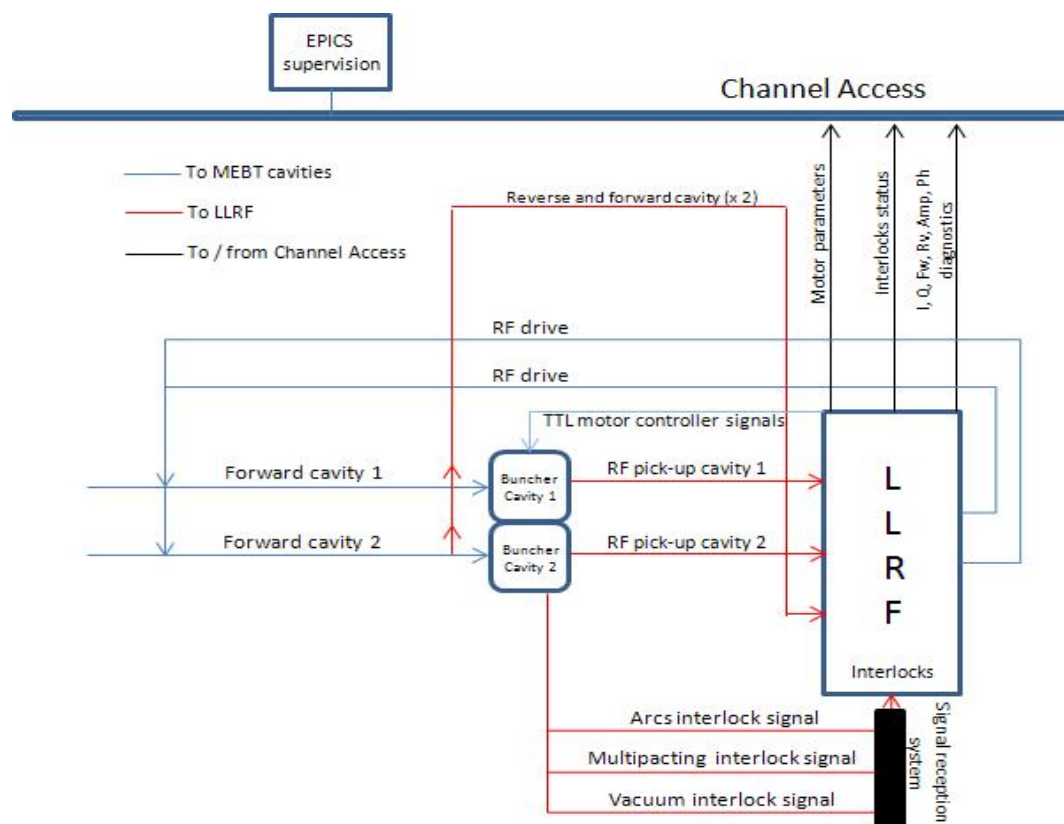


Figure 6.17: Signals interface between MEBT and LLRF

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# 7

## Prototype Test

*Las máquinas me sorprenden con mucha frecuencia.*

Alan Turing

### 7.1 Introduction

Given the complexity both the RF system and the LLRF system, designing a test bench and a prototype that cover both systems and their control is believed the most convenient option. Overcoming technological challenges that both systems hold, would mean a clear possibility to develop other systems with a greater chance of success. It is also important to re-emphasize that both the RF system as the LLRF have interfaces with almost all accelerator subsystems, therefore, a thorough understanding of the design and operation of both systems facilitates the work for the further development of other accelerator components.

This chapter shows the tests that have been conducted both for the LLRF system test bench and for the RF prototype chain with the LLRF system installed on it. To perform these tests, the LLRF system and the prototype chain have been operated through the LLRF and RF control systems explained in the previous chapters. These tests are, therefore, useful to test both the system itself and the functionality of the control system, taking into account that the system and its control are a whole, an inseparable unit. Through its control, all the parameters can be modified and the whole system can be operated and diagnosed.

The description of the tests passed to the LLRF system test bench, working without the amplifier chain, are shown in section [7.2](#). Tests on the RF Prototype Amplifier Chain are shown in [7.3](#).



## 7.2 LLRF system test bench

The LLRF system test bench, see Fig 7.1, was on first stage, installed and tested alone. Specific tests were necessary to have it completely ready to be integrated in the RF prototype chain.

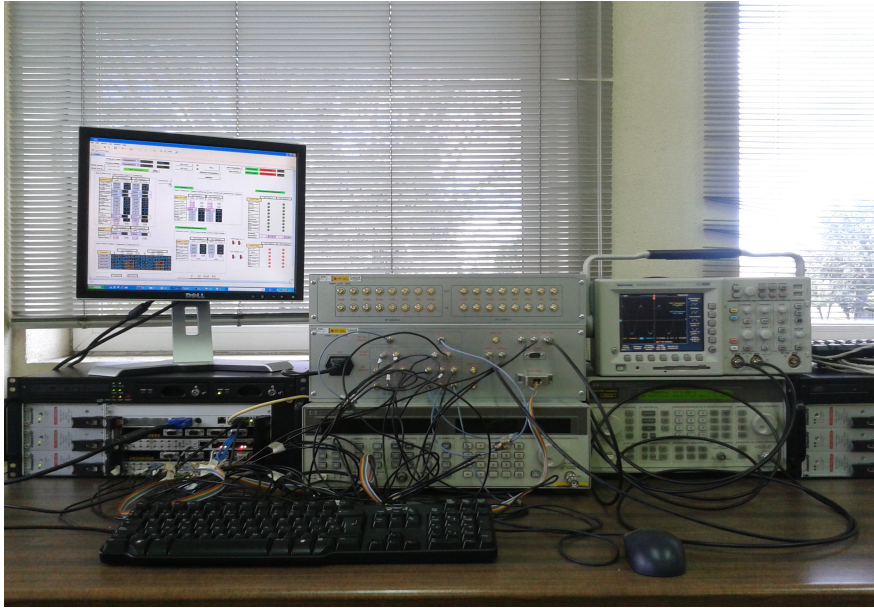


Figure 7.1: Image of LLRF test bench used in the tests explained in the next sections. Besides the components explained below, an oscilloscope employed to show the RF signal generated can be seen

The LLRF test bench consists of a RF generator, the LLRF itself and an oscilloscope. The RF generator provides a 175MHz, 18dBm signal to upconvert the DC control outputs of the digital board. The RF upconverted outputs are sent to a filter and a splitter, and from there, the RF signals are sent to the ADCs of the digital board to test the acquisition, the loops and the communications of the system. The reference output of the RF generator (10MHz) is used to synchronize the LLRF with the RF generator utilizing a PLL board installed in the front end of the LLRF.

As explained in previous sections, LLRF system interacts directly with RFQ, SRF Linac and MEBT, each subsystem has different characteristics and different interfaces with the LLRF system. In spite of these dissimilarities, the developed EPICS based control system in the LLRF is mostly the same for all three subsystems, i.e., there is a common LLRF control system development but with a few different PVs and a slightly different mode of operation depending the subsystem it interacts with. LLRF control software used for the following tests could successfully work for the essential functions in any of the mentioned subsystems, except for the plunger movement test in section 7.2.1.4, which is specially developed for MEBT subsystem.



### 7.2.1 LLRF control system software performance tests

Tests in this section ranging from EPICS operation itself to control system behavior, i.e., IOC launch checking, PVs on the Channel Access, interface operation, latency time and PVs interaction. They are explained in sections 7.2.1.1, 7.2.1.2, 7.2.1.3 and 7.2.1.4. The expected results for these tests are around to achieve complete communication between all layers of the control system within the range of microseconds. The transmission of information in the control system should not add extra time in any operation carried out in the accelerator. In addition, it is expected that the control system properly executes its configuration and diagnostics functions in the hypothetical situations simulated for these cases.

#### 7.2.1.1 EPICS process variables (PVs) test

The main and first test that an EPICS control system must pass relates to their process variables (PVs). The initial step is to successfully launch the corresponding IOC, without errors and with a good connection between the records database, the record support layer and the low level device driver. The execution of the IOC with satisfactory results can be seen in Fig. 7.3. The st.cmd file that configures the device features is loaded correctly, no errors appear. Loops and Diagnostics cards have been detected in their corresponding slot and they have been properly programmed. The clock is defined by default as external and a macro for PV names is accurately defined as *RF:LLRF*, which is used to unequivocally name all the PVs of the LLRF control system. Autosave module is also defined with its corresponding files and the storage frequency is settled to 5 seconds, i.e., samples of certain parameters are sent to a file every 5 seconds. The appearance of the EPICS prompt indicates that the initial run was successful and the communication with detected cards is possible now.

```

C:\Epics\applications\lyrtech\iocBoot\iocdrvLyrtechUhs>..\bin\win32-x86\drvLyrtechUhs.exe st.cmd
dbLoadDatabase("../db/drvLyrtechUhs.db")
drvLyrtechUhs_registerRecordDeviceDriver(pdbbase)
# Turn on asynTraceFlow and asynTraceError for global trace, i.e. no connected asynUser.
#asynSetTraceMask("", 0, 17)
drvLyrtechUhsConfigure("d1UHS", 1000)

Board UHS-ADC-8/16 found! -> Slot IDI01
Board UHS-ADC-8/16 found! -> Slot IDI11
2 UHS boards detected!!!

-----
Displaying UHS-ADAC Info...
-----

FPGA Programming Loops...SUCCESS!!!Press enter
Clock is External
FPGA Programming Diagnostics...SUCCESS!!!Press enter
Clock is External
Presione una tecla para continuar . . .
dbLoadRecords("../db/drvLyrtechUhs.db", "P=RF:,R=LLRF_,PORT=d1UHS,ADDR=0,TIMEOUT=1,NPOINTS=1000")
#asynSetTraceMask("d1UHS", 0, 0xff)
#asynSetTraceIOMask("d1UHS", 0, 0x2)
#set_requestfile_path("C:/EpicsR3.14.11/applications/iocBoot")
#set_savefile_path("C:/EpicsR3.14.11/applications/iocBoot")
#set_pass1_restoreFile(auto_settings.sav)
#save_restoreSet_DatedBackupFiles(1)
iocInit()
Starting iocInit
#####
## EPICS R3.14.11 $R3-14-11$ $2009/08/28 18:47:36$
## EPICS Base built Jun 27 2013
#####
iocRun: All initialization complete
# save other things every five seconds
#create_monitor_set("auto_settings.req", 5, "P=RF:", "R=LLRF")
epics>

```

Figure 7.2: Image of the IOC successfully launched for the LLRF control system

CA Simbólico del sistema de Visual Studio 2008 - ...\..\bin\win32-x86drv	CA Simbólico del sistema de Visual Studio 2008 - ...\..\bin\win32-x86drv
epics> dbl	RF:LLRF_CAUA:Uo1Rdbbk
RF:LLRF_CAUA:1kiRdbbk	RF:LLRF_CAUA:IctrlActionRdbbk
RF:LLRF_CAUA:AErrAccRdbbk	RF:LLRF_CAUA:Iendt1Rdbbk
RF:LLRF_CAUA:AErrPropRdbbk	RF:LLRF_CAUA:Iendt2Rdbbk
RF:LLRF_CAUA:AFrqTunCr1Rdbbk	RF:LLRF_CAUA:IffconRdbbk
RF:LLRF_CAUA:AREfRdbbk	RF:LLRF_CAUA:IfferrRdbbk
RF:LLRF_CAUA:AREfDb	RF:LLRF_CAUA:Ifw1AmpRdbbk
RF:LLRF_CAUA:ATunDPPhaseRdbbk	RF:LLRF_CAUA:Ifw2AmpRdbbk
RF:LLRF_CAUA:Au01Rdbbk	RF:LLRF_CAUA:Ifw3AmpRdbbk
RF:LLRF_CAUA:Au01db	RF:LLRF_CAUA:IfwCircRdbbk
RF:LLRF_CAUA:ActrlActionRdbbk	RF:LLRF_CAUA:IfwLoadRdbbk
RF:LLRF_CAUA:ActrlActionDb	RF:LLRF_CAUA:Ifw01Rdbbk
RF:LLRF_CAUA:AdcsHiftRdbbk	RF:LLRF_CAUA:IlkDiagArcs
RF:LLRF_CAUA:Aendt1Rdbbk	RF:LLRF_CAUA:IlkDiagCirc
RF:LLRF_CAUA:Aendt1db	RF:LLRF_CAUA:IlkDiagDAC
RF:LLRF_CAUA:Aendt2Rdbbk	RF:LLRF_CAUA:IlkDiagExtIlk
RF:LLRF_CAUA:Aendt2db	RF:LLRF_CAUA:IlkDiagFDL
RF:LLRF_CAUA:AffconRdbbk	RF:LLRF_CAUA:IlkDiagMPS
RF:LLRF_CAUA:Affc0ndb	RF:LLRF_CAUA:IlkDiagMPSInp
RF:LLRF_CAUA:AfferrRdbbk	RF:LLRF_CAUA:IlkDiagMult
RF:LLRF_CAUA:Afferrdb	RF:LLRF_CAUA:IlkDiagPLC
RF:LLRF_CAUA:Afwi1AmpRdbbk	RF:LLRF_CAUA:IlkDiagPin
RF:LLRF_CAUA:Afwi1Ampdb	RF:LLRF_CAUA:IlkDiagRevU
RF:LLRF_CAUA:Afwi2AmpRdbbk	RF:LLRF_CAUA:IlkDiagSpare
RF:LLRF_CAUA:Afwi2Ampdb	RF:LLRF_CAUA:IlkDiagSpareInp
RF:LLRF_CAUA:Afwi3AmpRdbbk	RF:LLRF_CAUA:IlkDiagVac
RF:LLRF_CAUA:Afwi3Amp3db	RF:LLRF_CAUA:IlkFwLoadRdbbk
RF:LLRF_CAUA:AfwiCavRdbbk	RF:LLRF_CAUA:IlkRvCavRdbbk
RF:LLRF_CAUA:AfwiCircRdbbk	RF:LLRF_CAUA:IlkRvCircRdbbk
RF:LLRF_CAUA:AfwiCircdb	RF:LLRF_CAUA:Irv0AmpRdbbk
RF:LLRF_CAUA:AfwiLoadRdbbk	RF:LLRF_CAUA:Irv0Amp3Rdbbk
RF:LLRF_CAUA:AfwiLoaddb	RF:LLRF_CAUA:IrvCircRdbbk
RF:LLRF_CAUA:Afwi01Rdbbk	RF:LLRF_CAUA:Irv01Rdbbk
RF:LLRF_CAUA:Afwi01db	RF:LLRF_CAUA:IspaceRdbbk
RF:LLRF_CAUA:AmprfminRdbbk	RF:LLRF_CAUA:KiRdbbk
RF:LLRF_CAUA:AmpsPareRdbbk	RF:LLRF_CAUA:KpRdbbk
RF:LLRF_CAUA:AmpsParedb	RF:LLRF_CAUA:LimRdbbk
RF:LLRF_CAUA:Angcav1Rdbbk	RF:LLRF_CAUA:LookrefmRdbbk
RF:LLRF_CAUA:AngfwrRdbbk	RF:LLRF_CAUA:MarginlowRdbbk
RF:LLRF_CAUA:Arw2AmpRdbbk	RF:LLRF_CAUA:MarginupRdbbk
RF:LLRF_CAUA:Arw2Ampdb	RF:LLRF_CAUA:Ma1uRdbbk
RF:LLRF_CAUA:Arw3Amp3Rdbbk	RF:LLRF_CAUA:Maxse1Rdbbk
RF:LLRF_CAUA:Arw3Amp3db	RF:LLRF_CAUA:Ma1uRdbbk
RF:LLRF_CAUA:ArwCircRdbbk	RF:LLRF_CAUA:Ma1uRdbbk
RF:LLRF_CAUA:ArwCircdb	RF:LLRF_CAUA:NumStepsRdbbk
RF:LLRF_CAUA:Arw01Rdbbk	RF:LLRF_CAUA:OnExtRefRdbbk
RF:LLRF_CAUA:Arw01db	RF:LLRF_CAUA:On1lkinArcsRdbbk
RF:LLRF_CAUA:CavampRdbbk	RF:LLRF_CAUA:On1lkinFwLoadRdbbk
RF:LLRF_CAUA:CauphRdbbk	RF:LLRF_CAUA:On1lkinMPSRdbbk
RF:LLRF_CAUA:CpDb1Rdbbk	RF:LLRF_CAUA:On1lkinManualRdbbk
RF:LLRF_CAUA:DCycleRdbbk	RF:LLRF_CAUA:On1lkinMu1Rdbbk
RF:LLRF_CAUA:DacshiftRdbbk	RF:LLRF_CAUA:On1lkinRvCavRdbbk
RF:LLRF_CAUA:ExternalOffRdbbk	RF:LLRF_CAUA:On1lkinRvCircRdbbk
RF:LLRF_CAUA:FidTotal	RF:LLRF_CAUA:On1lkinSpareRdbbk
RF:LLRF_CAUA:FiltercavRdbbk	RF:LLRF_CAUA:On1lkinVacRdbbk
RF:LLRF_CAUA:FreqTunLinRdbbk	RF:LLRF_CAUA:On1lkinManualRdbbk
RF:LLRF_CAUA:FreqSquareRdbbk	RF:LLRF_CAUA:On1lkinOuDACRdbbk
RF:LLRF_CAUA:FwminRdbbk	RF:LLRF_CAUA:On1lkinOuFd1Rdbbk
RF:LLRF_CAUA:Gain10Rdbbk	RF:LLRF_CAUA:On1lkinMPSRdbbk
RF:LLRF_CAUA:Gain11Rdbbk	RF:LLRF_CAUA:On1lkinOuPLCRdbbk
RF:LLRF_CAUA:Gain12Rdbbk	RF:LLRF_CAUA:On1lkinOuPinRdbbk
RF:LLRF_CAUA:Gain13Rdbbk	RF:LLRF_CAUA:On1lkinOuSprRdbbk
RF:LLRF_CAUA:Gain14Rdbbk	RF:LLRF_CAUA:OnMixerRdbbk
RF:LLRF_CAUA:Gain15Rdbbk	RF:LLRF_CAUA:PhasADCrdbk
RF:LLRF_CAUA:Gain16Rdbbk	RF:LLRF_CAUA:PhasDACrdbk
RF:LLRF_CAUA:Gain1Rdbbk	RF:LLRF_CAUA:PhasErrAccRdbbk
RF:LLRF_CAUA:Gain2Rdbbk	RF:LLRF_CAUA:PhasErrPropRdbbk
RF:LLRF_CAUA:Gain3Rdbbk	RF:LLRF_CAUA:PhasRdbbk
RF:LLRF_CAUA:Gain4Rdbbk	RF:LLRF_CAUA:PhasRefRdbbk
RF:LLRF_CAUA:Gain5Rdbbk	RF:LLRF_CAUA:PhasUo1Rdbbk
RF:LLRF_CAUA:Gain6Rdbbk	RF:LLRF_CAUA:PhasctrlActRdbbk
RF:LLRF_CAUA:Gain7Rdbbk	RF:LLRF_CAUA:PhaseoffRdbbk
RF:LLRF_CAUA:Gain8Rdbbk	RF:LLRF_CAUA:PhaserefminRdbbk
RF:LLRF_CAUA:Gain9Rdbbk	RF:LLRF_CAUA:PhasespareRdbbk
RF:LLRF_CAUA:Gain0LRdbbk	RF:LLRF_CAUA:Phasfwi1AmpRdbbk
RF:LLRF_CAUA:IErrAccRdbbk	RF:LLRF_CAUA:Phasfwi2AmpRdbbk
RF:LLRF_CAUA:IErrPropRdbbk	RF:LLRF_CAUA:Phasfwi3AmpRdbbk
RF:LLRF_CAUA:IRefRdbbk	RF:LLRF_CAUA:PhasfwiCavRdbbk
RF:LLRF_CAUA:Ilo1Rdbbk	RF:LLRF_CAUA:PhasfwiCircRdbbk
	RF:LLRF_CAUA:PhasfwiLoadRdbbk

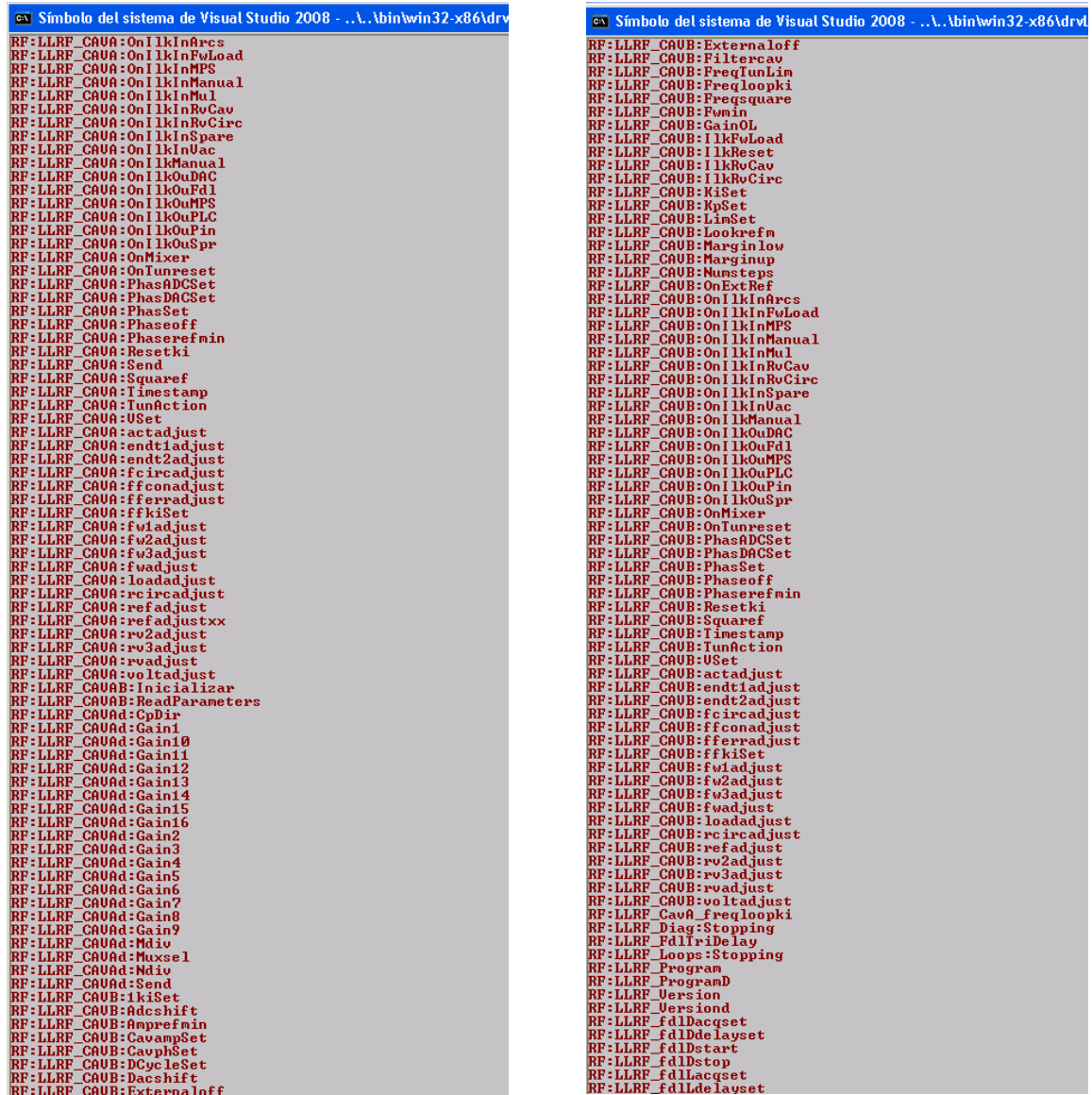
Figure 7.3: LLRF PVs running on the Channel Access and listed after the execution of the *dblist* command on the EPICS prompt

RF:LLRF\_CAUB:Affcandb  
RF:LLRF\_CAUB:AfferrRdbk  
RF:LLRF\_CAUB:Afferrdb  
RF:LLRF\_CAUB:Afw1AmpRdbk  
RF:LLRF\_CAUB:Afw1Ampdb  
RF:LLRF\_CAUB:Afw2AmpRdbk  
RF:LLRF\_CAUB:Afw2Ampdb  
RF:LLRF\_CAUB:Afwamp3Rdbk  
RF:LLRF\_CAUB:Afwamp3db  
RF:LLRF\_CAUB:AfwCavRdbk  
RF:LLRF\_CAUB:AfwCircRdbk  
RF:LLRF\_CAUB:AfwCircdb  
RF:LLRF\_CAUB:AfwLoadRdbk  
RF:LLRF\_CAUB:AfwLoaddb  
RF:LLRF\_CAUB:AfwUo1Rdbk  
RF:LLRF\_CAUB:AfwUo1db  
RF:LLRF\_CAUB:AmprefminRdbk  
RF:LLRF\_CAUB:Amps pareRdbk  
RF:LLRF\_CAUB:Amps paredb  
RF:LLRF\_CAUB:Arv2AmpRdbk  
RF:LLRF\_CAUB:Arv2Ampdb  
RF:LLRF\_CAUB:Arvamp3Rdbk  
RF:LLRF\_CAUB:Arvamp3db  
RF:LLRF\_CAUB:ArvCircRdbk  
RF:LLRF\_CAUB:ArvCircdb  
RF:LLRF\_CAUB:ArvUo1Rdbk  
RF:LLRF\_CAUB:ArvUo1db  
RF:LLRF\_CAUB:CavampRdbk  
RF:LLRF\_CAUB:CavphRdbk  
RF:LLRF\_CAUB:DCycleRdbk  
RF:LLRF\_CAUB:Dacshiftrdbk  
RF:LLRF\_CAUB:ExternaloffRdbk  
RF:LLRF\_CAUB:FiIdTotal  
RF:LLRF\_CAUB:FiItercavRdbk  
RF:LLRF\_CAUB:FreqTunLimRdbk  
RF:LLRF\_CAUB:FreqloopkiRdbk  
RF:LLRF\_CAUB:FreqsquareRdbk  
RF:LLRF\_CAUB:FwminRdbk  
RF:LLRF\_CAUB:GainOLRdbk  
RF:LLRF\_CAUB:IErrAccRdbk  
RF:LLRF\_CAUB:IErrPropRdbk  
RF:LLRF\_CAUB:IRefRdbk  
RF:LLRF\_CAUB:Uo1Rdbk  
RF:LLRF\_CAUB:ICtrIfectionRdbk  
RF:LLRF\_CAUB:Iendt1Rdbk  
RF:LLRF\_CAUB:Iendt2Rdbk  
RF:LLRF\_CAUB:IffconRdbk  
RF:LLRF\_CAUB:IfferrRdbk  
RF:LLRF\_CAUB:Ifw1AmpRdbk  
RF:LLRF\_CAUB:Ifw2AmpRdbk  
RF:LLRF\_CAUB:Ifwamp3Rdbk  
RF:LLRF\_CAUB:IfwCircRdbk  
RF:LLRF\_CAUB:IfwLoadRdbk  
RF:LLRF\_CAUB:IfwUo1Rdbk  
RF:LLRF\_CAUB:IlkDiagfres  
RF:LLRF\_CAUB:IlkDiagCirc  
RF:LLRF\_CAUB:IlkDiagD4C  
RF:LLRF\_CAUB:IlkDiagExtIlk  
RF:LLRF\_CAUB:IlkDiagFDL  
RF:LLRF\_CAUB:IlkDiagMPS  
RF:LLRF\_CAUB:IlkDiagMPSInp  
RF:LLRF\_CAUB:IlkDiagMult  
RF:LLRF\_CAUB:IlkDiagPLC  
RF:LLRF\_CAUB:IlkDiagPin  
RF:LLRF\_CAUB:IlkDiagRevU  
RF:LLRF\_CAUB:IlkDiagSpare  
RF:LLRF\_CAUB:IlkDiagSpareInp  
RF:LLRF\_CAUB:IlkDiagVac  
RF:LLRF\_CAUB:IlkFwLoadRdbk  
RF:LLRF\_CAUB:IlkRvCavRdbk  
RF:LLRF\_CAUB:IlkRvCircRdbk  
RF:LLRF\_CAUB:Irv2AmpRdbk  
RF:LLRF\_CAUB:Irvamp3Rdbk  
RF:LLRF\_CAUB:IrvCircRdbk  
RF:LLRF\_CAUB:IrvUo1Rdbk  
RF:LLRF\_CAUB:IspareRdbk  
RF:LLRF\_CAUB:KiRdbk  
RF:LLRF\_CAUB:KpRdbk  
RF:LLRF\_CAUB:limRdbk

Figure 7.4: LLRF PVs running on the Channel Access and listed after the execution of the *db/l* command on the EPICS prompt. II

cn Símbolo del sistema de Visual Studio 2008 - ..\..\bin\win32-x86\drv	cn Símbolo del sistema de Visual Studio 2008 - ..\..\bin\win32-x86\drv
RF:LLRF_CAUB:LinRdbk	RF:LLRF_Diag:Over10
RF:LLRF_CAUB:LookrefnRdbk	RF:LLRF_Diag:Over11
RF:LLRF_CAUB:MarginlowRdbk	RF:LLRF_Diag:Over12
RF:LLRF_CAUB:MarginupRdbk	RF:LLRF_Diag:Over13
RF:LLRF_CAUB:MunstepsRdbk	RF:LLRF_Diag:Over14
RF:LLRF_CAUB:OnExtRefRdbk	RF:LLRF_Diag:Over15
RF:LLRF_CAUB:OnIlkInArCsRdbk	RF:LLRF_Diag:Over16
RF:LLRF_CAUB:OnIlkInFwLoadRdbk	RF:LLRF_Diag:Over2
RF:LLRF_CAUB:OnIlkInMPSRdbk	RF:LLRF_Diag:Over3
RF:LLRF_CAUB:OnIlkInManualRdbk	RF:LLRF_Diag:Over4
RF:LLRF_CAUB:OnIlkInMu1Rdbk	RF:LLRF_Diag:Over5
RF:LLRF_CAUB:OnIlkInRuCavRdbk	RF:LLRF_Diag:Over6
RF:LLRF_CAUB:OnIlkInRuCircRdbk	RF:LLRF_Diag:Over7
RF:LLRF_CAUB:OnIlkInSpareRdbk	RF:LLRF_Diag:Over8
RF:LLRF_CAUB:OnIlkInVacRdbk	RF:LLRF_Diag:Over9
RF:LLRF_CAUB:OnIlkManualRdbk	RF:LLRF_Diag:OverA11
RF:LLRF_CAUB:OnIlkOuDACRdbk	RF:LLRF_Loops:Over1
RF:LLRF_CAUB:OnIlkOuFd1Rdbk	RF:LLRF_Loops:Over2
RF:LLRF_CAUB:OnIlkOuMPSRdbk	RF:LLRF_Loops:Over3
RF:LLRF_CAUB:OnIlkOuPLCRdbk	RF:LLRF_Loops:Over4
RF:LLRF_CAUB:OnIlkOuPinRdbk	RF:LLRF_Loops:Over5
RF:LLRF_CAUB:OnIlkOuSprRdbk	RF:LLRF_Loops:Over6
RF:LLRF_CAUB:OnMixerRdbk	RF:LLRF_Loops:Over7
RF:LLRF_CAUB:PhasADCRdbk	RF:LLRF_Loops:Over8
RF:LLRF_CAUB:PhasDACRdbk	RF:LLRF_Loops:OverA11
RF:LLRF_CAUB:PhasErrAccRdbk	RF:LLRF_VersionRdbk
RF:LLRF_CAUB:PhasErrPropRdbk	RF:LLRF_VersiondRdbk
RF:LLRF_CAUB:PhasRefRdbk	RF:LLRF_fdlDelayRdbk
RF:LLRF_CAUB:PhasUo1Rdbk	RF:LLRF_fdlDelayRdbk
RF:LLRF_CAUB:Phasctr1ActRdbk	RF:LLRF_CAUA:1kiSet
RF:LLRF_CAUB:PhaseoffRdbk	RF:LLRF_CAUA:Adcshift
RF:LLRF_CAUB:PhaserefminRdbk	RF:LLRF_CAUA:Amprfmin
RF:LLRF_CAUB:PhasespareRdbk	RF:LLRF_CAUA:CavampSet
RF:LLRF_CAUB:Phasfw1AmpRdbk	RF:LLRF_CAUA:CauphSet
RF:LLRF_CAUB:Phasfw2AmpRdbk	RF:LLRF_CAUA:CpDir
RF:LLRF_CAUB:PhasfwAmp3Rdbk	RF:LLRF_CAUA:DcycleSet
RF:LLRF_CAUB:PhasfwCavRdbk	RF:LLRF_CAUA:Dacshift
RF:LLRF_CAUB:PhasfwCircRdbk	RF:LLRF_CAUA:Externaloff
RF:LLRF_CAUB:PhasfwLoadRdbk	RF:LLRF_CAUA:Filtercav
RF:LLRF_CAUB:PhasfwUo1Rdbk	RF:LLRF_CAUA:FreqTunLim
RF:LLRF_CAUB:Phasru2AmpRdbk	RF:LLRF_CAUA:Freqsquare
RF:LLRF_CAUB:PhasruAmp3Rdbk	RF:LLRF_CAUA:Fwmin
RF:LLRF_CAUB:PhasruCircRdbk	RF:LLRF_CAUA:Gain1
RF:LLRF_CAUB:PhasruUo1Rdbk	RF:LLRF_CAUA:Gain10
RF:LLRF_CAUB:Phendt1Rdbk	RF:LLRF_CAUA:Gain11
RF:LLRF_CAUB:Phendt2Rdbk	RF:LLRF_CAUA:Gain12
RF:LLRF_CAUB:PhffconRdbk	RF:LLRF_CAUA:Gain13
RF:LLRF_CAUB:PhfferrRdbk	RF:LLRF_CAUA:Gain14
RF:LLRF_CAUB:QErrAccRdbk	RF:LLRF_CAUA:Gain15
RF:LLRF_CAUB:QErrPropRdbk	RF:LLRF_CAUA:Gain16
RF:LLRF_CAUB:QRefRdbk	RF:LLRF_CAUA:Gain1D
RF:LLRF_CAUB:QUo1Rdbk	RF:LLRF_CAUA:Gain1L
RF:LLRF_CAUB:Qctr1ActionRdbk	RF:LLRF_CAUA:Gain2
RF:LLRF_CAUB:Qendt1Rdbk	RF:LLRF_CAUA:Gain3
RF:LLRF_CAUB:Qendt2Rdbk	RF:LLRF_CAUA:Gain4
RF:LLRF_CAUB:QffconRdbk	RF:LLRF_CAUA:Gain5
RF:LLRF_CAUB:QfferrRdbk	RF:LLRF_CAUA:Gain6
RF:LLRF_CAUB:Qfw1AmpRdbk	RF:LLRF_CAUA:Gain7
RF:LLRF_CAUB:Qfw2AmpRdbk	RF:LLRF_CAUA:Gain8
RF:LLRF_CAUB:QfwAmp3Rdbk	RF:LLRF_CAUA:Gain9
RF:LLRF_CAUB:QfwCircRdbk	RF:LLRF_CAUA:Gain9D
RF:LLRF_CAUB:QfwLoadRdbk	RF:LLRF_CAUA:Gain9L
RF:LLRF_CAUB:QfwUo1Rdbk	RF:LLRF_CAUA:GainOL
RF:LLRF_CAUB:Qru2AmpRdbk	RF:LLRF_CAUA:IlkFwLoad
RF:LLRF_CAUB:QruAmp3Rdbk	RF:LLRF_CAUA:IlkReset
RF:LLRF_CAUB:QruCircRdbk	RF:LLRF_CAUA:IlkRuCav
RF:LLRF_CAUB:QruUo1Rdbk	RF:LLRF_CAUA:IlkRuCirc
RF:LLRF_CAUB:QspareRdbk	RF:LLRF_CAUA:KiSet
RF:LLRF_CAUB:ResetkiRdbk	RF:LLRF_CAUA:KpSet
RF:LLRF_CAUB:SquarefRdbk	RF:LLRF_CAUA:LinSet
RF:LLRF_CAUB:TunActionRdbk	RF:LLRF_CAUA:Lookrefm
RF:LLRF_CAUB:URdbk	RF:LLRF_CAUA:Marginlow
RF:LLRF_CAUB:ffkiRdbk	RF:LLRF_CAUA:Marginup
RF:LLRF_CAUB:stampRdbk	RF:LLRF_CAUA:Mdiv
RF:LLRF_CAUBmodb	RF:LLRF_CAUA:Muxsel
RF:LLRF_CavA_freqloopki_RBU	RF:LLRF_CAUA:Ndiv
RF:LLRF_Diag:Over1	RF:LLRF_CAUA:Munsteps
RF:LLRF_Diag:Over10	RF:LLRF_CAUA:OnExtRef
	RF:LLRF_CAUA:OnIlkInArCs

Figure 7.5: LLRF PVs running on the Channel Access and listed after the execution of the *dbI* command on the EPICS prompt, III



CA Símbolo del sistema de Visual Studio 2008 - ...\\bin\\win32-x86\\drv

RF:LLRF\_CAUA:OnIlkInArcs  
 RF:LLRF\_CAUA:OnIlkInFwLoad  
 RF:LLRF\_CAUA:OnIlkInMPS  
 RF:LLRF\_CAUA:OnIlkInManual  
 RF:LLRF\_CAUA:OnIlkInMul  
 RF:LLRF\_CAUA:OnIlkInRuCav  
 RF:LLRF\_CAUA:OnIlkInRuCirc  
 RF:LLRF\_CAUA:OnIlkInSpare  
 RF:LLRF\_CAUA:OnIlkInVac  
 RF:LLRF\_CAUA:OnIlkManual  
 RF:LLRF\_CAUA:OnIlkOuDAC  
 RF:LLRF\_CAUA:OnIlkOuFd1  
 RF:LLRF\_CAUA:OnIlkOuMPS  
 RF:LLRF\_CAUA:OnIlkOuPLC  
 RF:LLRF\_CAUA:OnIlkOuPin  
 RF:LLRF\_CAUA:OnIlkOuSpr  
 RF:LLRF\_CAUA:OnMixer  
 RF:LLRF\_CAUA:OnTunreset  
 RF:LLRF\_CAUA:PhasADCSet  
 RF:LLRF\_CAUA:PhasDACSet  
 RF:LLRF\_CAUA:PhasSet  
 RF:LLRF\_CAUA:Phaseoff  
 RF:LLRF\_CAUA:Phaserefmin  
 RF:LLRF\_CAUA:Resetki  
 RF:LLRF\_CAUA:Send  
 RF:LLRF\_CAUA:Squaref  
 RF:LLRF\_CAUA:Timestamp  
 RF:LLRF\_CAUA:TunAction  
 RF:LLRF\_CAUA:USet  
 RF:LLRF\_CAUA:actadjust  
 RF:LLRF\_CAUA:endt1adjust  
 RF:LLRF\_CAUA:endt2adjust  
 RF:LLRF\_CAUA:fcircadjust  
 RF:LLRF\_CAUA:ffconadjust  
 RF:LLRF\_CAUA:ffferadjust  
 RF:LLRF\_CAUA:ffkiSet  
 RF:LLRF\_CAUA:fw1adjust  
 RF:LLRF\_CAUA:fw2adjust  
 RF:LLRF\_CAUA:fw3adjust  
 RF:LLRF\_CAUA:fwadjust  
 RF:LLRF\_CAUA:loadadjust  
 RF:LLRF\_CAUA:rcircadjust  
 RF:LLRF\_CAUA:refadjust  
 RF:LLRF\_CAUA:refadjustxx  
 RF:LLRF\_CAUA:rv2adjust  
 RF:LLRF\_CAUA:rv3adjust  
 RF:LLRF\_CAUA:rvadjust  
 RF:LLRF\_CAUA:voltadjust  
 RF:LLRF\_CAUB:Inicializar  
 RF:LLRF\_CAUB:ReadParameters  
 RF:LLRF\_CAUB:CPDir  
 RF:LLRF\_CAUB:Gain1  
 RF:LLRF\_CAUB:Gain10  
 RF:LLRF\_CAUB:Gain11  
 RF:LLRF\_CAUB:Gain12  
 RF:LLRF\_CAUB:Gain13  
 RF:LLRF\_CAUB:Gain14  
 RF:LLRF\_CAUB:Gain15  
 RF:LLRF\_CAUB:Gain16  
 RF:LLRF\_CAUB:Gain2  
 RF:LLRF\_CAUB:Gain3  
 RF:LLRF\_CAUB:Gain4  
 RF:LLRF\_CAUB:Gain5  
 RF:LLRF\_CAUB:Gain6  
 RF:LLRF\_CAUB:Gain7  
 RF:LLRF\_CAUB:Gain8  
 RF:LLRF\_CAUB:Gain9  
 RF:LLRF\_CAUB:Mdiv  
 RF:LLRF\_CAUB:Muxsel  
 RF:LLRF\_CAUB:Mdiv  
 RF:LLRF\_CAUB:Send  
 RF:LLRF\_CAUB:1kiSet  
 RF:LLRF\_CAUB:Adcshift  
 RF:LLRF\_CAUB:Amprfmin  
 RF:LLRF\_CAUB:CavampSet  
 RF:LLRF\_CAUB:CavphSet  
 RF:LLRF\_CAUB:DCycleSet  
 RF:LLRF\_CAUB:Dacshift  
 RF:LLRF\_CAUB:Externaloff

CA Símbolo del sistema de Visual Studio 2008 - ...\\bin\\win32-x86\\drv

RF:LLRF\_CAUB:Externaloff  
 RF:LLRF\_CAUB:Filtercav  
 RF:LLRF\_CAUB:FreqTunLin  
 RF:LLRF\_CAUB:Freqloopki  
 RF:LLRF\_CAUB:Freqsquare  
 RF:LLRF\_CAUB:Fomin  
 RF:LLRF\_CAUB:Gain0L  
 RF:LLRF\_CAUB:IlkFwLoad  
 RF:LLRF\_CAUB:IlkReset  
 RF:LLRF\_CAUB:IlkRuCav  
 RF:LLRF\_CAUB:IlkRuCirc  
 RF:LLRF\_CAUB:KiSet  
 RF:LLRF\_CAUB:KpSet  
 RF:LLRF\_CAUB:LimSet  
 RF:LLRF\_CAUB:Lookrefm  
 RF:LLRF\_CAUB:Marginlow  
 RF:LLRF\_CAUB:Marginup  
 RF:LLRF\_CAUB:Numsteps  
 RF:LLRF\_CAUB:OnExtRef  
 RF:LLRF\_CAUB:OnIlkInArcs  
 RF:LLRF\_CAUB:OnIlkInFwLoad  
 RF:LLRF\_CAUB:OnIlkInMPS  
 RF:LLRF\_CAUB:OnIlkInManual  
 RF:LLRF\_CAUB:OnIlkInMul  
 RF:LLRF\_CAUB:OnIlkInRuCav  
 RF:LLRF\_CAUB:OnIlkInRuCirc  
 RF:LLRF\_CAUB:OnIlkInSpare  
 RF:LLRF\_CAUB:OnIlkInVac  
 RF:LLRF\_CAUB:OnIlkManual  
 RF:LLRF\_CAUB:OnIlkOuDAC  
 RF:LLRF\_CAUB:OnIlkOuFd1  
 RF:LLRF\_CAUB:OnIlkOuMPS  
 RF:LLRF\_CAUB:OnIlkOuPLC  
 RF:LLRF\_CAUB:OnIlkOuPin  
 RF:LLRF\_CAUB:OnIlkOuSpr  
 RF:LLRF\_CAUB:OnMixer  
 RF:LLRF\_CAUB:OnTunreset  
 RF:LLRF\_CAUB:PhasADCSet  
 RF:LLRF\_CAUB:PhasDACSet  
 RF:LLRF\_CAUB:PhasSet  
 RF:LLRF\_CAUB:Phaseoff  
 RF:LLRF\_CAUB:Phaserefmin  
 RF:LLRF\_CAUB:Resetki  
 RF:LLRF\_CAUB:Squaref  
 RF:LLRF\_CAUB:Timestamp  
 RF:LLRF\_CAUB:TunAction  
 RF:LLRF\_CAUB:USet  
 RF:LLRF\_CAUB:actadjust  
 RF:LLRF\_CAUB:endt1adjust  
 RF:LLRF\_CAUB:endt2adjust  
 RF:LLRF\_CAUB:fcircadjust  
 RF:LLRF\_CAUB:ffconadjust  
 RF:LLRF\_CAUB:ffferadjust  
 RF:LLRF\_CAUB:ffkiSet  
 RF:LLRF\_CAUB:fw1adjust  
 RF:LLRF\_CAUB:fw2adjust  
 RF:LLRF\_CAUB:fw3adjust  
 RF:LLRF\_CAUB:fwadjust  
 RF:LLRF\_CAUB:loadadjust  
 RF:LLRF\_CAUB:rcircadjust  
 RF:LLRF\_CAUB:refadjust  
 RF:LLRF\_CAUB:rv2adjust  
 RF:LLRF\_CAUB:rv3adjust  
 RF:LLRF\_CAUB:rvadjust  
 RF:LLRF\_CAUB:voltadjust  
 RF:LLRF\_CAUB:freqloopki  
 RF:LLRF\_Diag:Stopping  
 RF:LLRF\_FdlIrDelay  
 RF:LLRF\_Loops:Stopping  
 RF:LLRF\_Program  
 RF:LLRF\_ProgramD  
 RF:LLRF\_Version  
 RF:LLRF\_VersionD  
 RF:LLRF\_fdlDacqset  
 RF:LLRF\_fdlDelayset  
 RF:LLRF\_fdlDstart  
 RF:LLRF\_fdlDstop  
 RF:LLRF\_fdlLacqset  
 RF:LLRF\_fdlDelayset

Figure 7.6: LLRF PVs running on the Channel Access and listed after the execution of the *dbf* command on the EPICS prompt, IV

CA Símbolo del sistema de Visual Studio 2008 - ...\bin\win32-x86\drv	CA Símbolo del sistema de Visual Studio 2008 - ...\bin\win32-x86\drv
RF:LLRF_fdlDdelayset	RF:LLRF_CAUA:OnTuningPos
RF:LLRF_fdlDstart	RF:LLRF_CAUA:OnUacIlk
RF:LLRF_fdlDstop	RF:LLRF_CAUA:Onffloop
RF:LLRF_fdlLacqset	RF:LLRF_CAUA:Onpulse
RF:LLRF_fdlLdelayset	RF:LLRF_CAUA:Plgauto
RF:LLRF_fdlLstart	RF:LLRF_CAUA:Plgmanual
RF:LLRF_fdlLstop	RF:LLRF_CAUA:Plgup
RF:LLRF_CAUA:AutoenableRdbk	RF:LLRF_CAUA:Uachig
RF:LLRF_CAUA:AutostartRdbk	RF:LLRF_CAUA:Uac low
RF:LLRF_CAUA:EpsdelayRdbk	RF:LLRF_CAUA:BlockParameters
RF:LLRF_CAUA:EpsdisableRdbk	RF:LLRF_CAUA:UnblockParameters
RF:LLRF_CAUA:FindelayRdbk	RF:LLRF_CAUA:Autostart
RF:LLRF_CAUA:FindisableRdbk	RF:LLRF_CAUA:Epsdelay
RF:LLRF_CAUA:OnFreqTunPosRdbk	RF:LLRF_CAUA:Epsdisable
RF:LLRF_CAUA:OnFreqTunRdbk	RF:LLRF_CAUA:Findelay
RF:LLRF_CAUA:OnLookRefRdbk	RF:LLRF_CAUA:Findisable
RF:LLRF_CAUA:OnLoopRdbk	RF:LLRF_CAUA:OnFreqTun
RF:LLRF_CAUA:OnManualFreqTunRdbk	RF:LLRF_CAUA:OnFreqTunPos
RF:LLRF_CAUA:OnMovePlgRdbk	RF:LLRF_CAUA:OnLookRef
RF:LLRF_CAUA:OnMoveupRdbk	RF:LLRF_CAUA:OnLoop
RF:LLRF_CAUA:OnPhasADCdbk	RF:LLRF_CAUA:OnManualFreqTun
RF:LLRF_CAUA:OnPhasDACdbk	RF:LLRF_CAUA:OnMovePlg
RF:LLRF_CAUA:OnPulsModeRdbk	RF:LLRF_CAUA:OnMoveup
RF:LLRF_CAUA:OnTuningPosRdbk	RF:LLRF_CAUA:OnPhasADC
RF:LLRF_CAUA:OnTuningRdbk	RF:LLRF_CAUA:OnPhasDAC
RF:LLRF_CAUA:OnUacIlkRdbk	RF:LLRF_CAUA:OnPulsMode
RF:LLRF_CAUA:OnffloopRdbk	RF:LLRF_CAUA:OnTuning
RF:LLRF_CAUA:OnpulseRdbk	RF:LLRF_CAUA:OnTuningPos
RF:LLRF_CAUA:PlgautoRdbk	RF:LLRF_CAUA:OnUacIlk
RF:LLRF_CAUA:PlgmanualRdbk	RF:LLRF_CAUA:Onffloop
RF:LLRF_CAUA:PlgupRdbk	RF:LLRF_CAUA:Onpulse
RF:LLRF_CAUA:UachigRdbk	RF:LLRF_CAUA:Plgauto
RF:LLRF_CAUA:Uac lowRdbk	RF:LLRF_CAUA:Plgmanual
RF:LLRF_CAUA:AutostartRdbk	RF:LLRF_CAUA:Plgup
RF:LLRF_CAUA:EpsdelayRdbk	RF:LLRF_CAUA:Uachig
RF:LLRF_CAUA:EpsdisableRdbk	RF:LLRF_CAUA:Uac low
RF:LLRF_CAUA:FindelayRdbk	RF:LLRF_CAUA:autoenable
RF:LLRF_CAUA:FindisableRdbk	RF:LLRF_ReadStatus
RF:LLRF_CAUA:OnFreqTunPosRdbk	RF:LLRF_block_parameters
RF:LLRF_CAUA:OnFreqTunRdbk	RF:LLRF_CAUA:ConstartRdbk
RF:LLRF_CAUA:OnLookRefRdbk	RF:LLRF_CAUA:Mux0Rdbk
RF:LLRF_CAUA:OnLoopRdbk	RF:LLRF_CAUA:Mux1Rdbk
RF:LLRF_CAUA:OnManualFreqTunRdbk	RF:LLRF_CAUA:Mux2Rdbk
RF:LLRF_CAUA:OnMovePlgRdbk	RF:LLRF_CAUA:Mux3Rdbk
RF:LLRF_CAUA:OnMoveupRdbk	RF:LLRF_CAUA:Mux4Rdbk
RF:LLRF_CAUA:OnPhasADCdbk	RF:LLRF_CAUA:PhincrateRdbk
RF:LLRF_CAUA:OnPhasDACdbk	RF:LLRF_CAUA:PulsesRdbk
RF:LLRF_CAUA:OnPulsModeRdbk	RF:LLRF_CAUA:QuadRdbk
RF:LLRF_CAUA:OnTuningPosRdbk	RF:LLRF_CAUA:SamplesRdbk
RF:LLRF_CAUA:OnTuningRdbk	RF:LLRF_CAUA:StagesRdbk
RF:LLRF_CAUA:OnUacIlkRdbk	RF:LLRF_CAUA:StstartRdbk
RF:LLRF_CAUA:OnffloopRdbk	RF:LLRF_CAUA:UIncRdbk
RF:LLRF_CAUA:OnpulseRdbk	RF:LLRF_CAUA:Mux0Rdbk
RF:LLRF_CAUA:PlgautoRdbk	RF:LLRF_CAUA:Mux1Rdbk
RF:LLRF_CAUA:PlgmanualRdbk	RF:LLRF_CAUA:Mux2Rdbk
RF:LLRF_CAUA:PlgupRdbk	RF:LLRF_CAUA:Mux3Rdbk
RF:LLRF_CAUA:UachigRdbk	RF:LLRF_CAUA:Mux4Rdbk
RF:LLRF_CAUA:Uac lowRdbk	RF:LLRF_CAUA:ConstartRdbk
RF:LLRF_CavB_autoenable_RBU	RF:LLRF_CAUA:PhincrateRdbk
RF:LLRF_fdlDtrigRdbk	RF:LLRF_CAUA:PulsesRdbk
RF:LLRF_fdlLtrigRdbk	RF:LLRF_CAUA:QuadRdbk
RF:LLRF_CAUA:Autoenable	RF:LLRF_CAUA:SamplesRdbk
RF:LLRF_CAUA:Autostart	RF:LLRF_CAUA:StagesRdbk
RF:LLRF_CAUA:Epsdelay	RF:LLRF_CAUA:StstartRdbk
RF:LLRF_CAUA:Epsdisable	RF:LLRF_CAUA:UIncRdbk
RF:LLRF_CAUA:Findelay	RF:LLRF_Diag:ClockRdbk
RF:LLRF_CAUA:Findisable	RF:LLRF_Diag:LockedRdbk
RF:LLRF_CAUA:OnFreqTun	RF:LLRF_Diag:RunningRdbk
RF:LLRF_CAUA:OnFreqTunPos	RF:LLRF_Loops:ClockRdbk
RF:LLRF_CAUA:OnLookRef	RF:LLRF_Loops:LockedRdbk
RF:LLRF_CAUA:OnLoop	RF:LLRF_Loops:RunningRdbk
RF:LLRF_CAUA:OnManualFreqTun	RF:LLRF_MensaRdbk
RF:LLRF_CAUA:OnMovePlg	RF:LLRF_CAUA:Constart
RF:LLRF_CAUA:OnMoveup	RF:LLRF_CAUA:Mux0
RF:LLRF_CAUA:OnPhasADC	RF:LLRF_CAUA:Mux1
RF:LLRF_CAUA:OnPhasDAC	RF:LLRF_CAUA:Mux2
RF:LLRF_CAUA:OnPulsMode	RF:LLRF_CAUA:Mux3
RF:LLRF_CAUA:OnTuning	RF:LLRF_CAUA:Mux4
RF:LLRF_CAUA:OnTuningPos	RF:LLRF_CAUA:Phincrate

Figure 7.7: LLRF PVs running on the Channel Access and listed after the execution of the *db/* command on the EPICS prompt, V

```

Símbolo del sistema de Visual Studio 2008 - ...\bin\win32-x86\drv
RF:LLRF_CAUB:OnTuning
RF:LLRF_CAUB:OnTuningPos
RF:LLRF_CAUB:OnVac1lk
RF:LLRF_CAUB:Onffloop
RF:LLRF_CAUB:Onpulse
RF:LLRF_CAUB:Plgauto
RF:LLRF_CAUB:Plgmanual
RF:LLRF_CAUB:Plgup
RF:LLRF_CAUB:Uachig
RF:LLRF_CAUB:Uaclo
RF:LLRF_CavB_autoenable
RF:LLRF_ReadStatus
RF:LLRF_block_parameters
RF:LLRF_CAUA:ComstartRdbk
RF:LLRF_CAUA:Mux0Rdbk
RF:LLRF_CAUA:Mux1Rdbk
RF:LLRF_CAUA:Mux2Rdbk
RF:LLRF_CAUA:Mux3Rdbk
RF:LLRF_CAUA:Mux4Rdbk
RF:LLRF_CAUA:PhincrateRdbk
RF:LLRF_CAUA:PulsesRdbk
RF:LLRF_CAUA:QuadRdbk
RF:LLRF_CAUA:SamplesRdbk
RF:LLRF_CAUA:StagesRdbk
RF:LLRF_CAUA:StstartRdbk
RF:LLRF_CAUA:UIncRdbk
RF:LLRF_CAUA:Mux0Rdbk
RF:LLRF_CAUA:Mux1Rdbk
RF:LLRF_CAUA:Mux2Rdbk
RF:LLRF_CAUA:Mux3Rdbk
RF:LLRF_CAUA:Mux4Rdbk
RF:LLRF_CAUA:ComstartRdbk
RF:LLRF_CAUA:PhincrateRdbk
RF:LLRF_CAUA:PulsesRdbk
RF:LLRF_CAUA:QuadRdbk
RF:LLRF_CAUA:SamplesRdbk
RF:LLRF_CAUA:StagesRdbk
RF:LLRF_CAUA:StstartRdbk
RF:LLRF_CAUA:UIncRdbk
RF:LLRF_Diag:ClockRdbk
RF:LLRF_Diag:LockedRdbk
RF:LLRF_Diag:RunningRdbk
RF:LLRF_Loops:ClockRdbk
RF:LLRF_Loops:LockedRdbk
RF:LLRF_Loops:RunningRdbk
RF:LLRF_MensaRdbk
RF:LLRF_CAUA:Comstart
RF:LLRF_CAUA:Mux0
RF:LLRF_CAUA:Mux1
RF:LLRF_CAUA:Mux2
RF:LLRF_CAUA:Mux3
RF:LLRF_CAUA:Mux4
RF:LLRF_CAUA:Phincrate
RF:LLRF_CAUA:Pulses
RF:LLRF_CAUA:QuadSet
RF:LLRF_CAUA:Samples
RF:LLRF_CAUA:Stages
RF:LLRF_CAUA:UIncSet
RF:LLRF_CAUA:Mux0
RF:LLRF_CAUA:Mux1
RF:LLRF_CAUA:Mux2
RF:LLRF_CAUA:Mux3
RF:LLRF_CAUA:Mux4
RF:LLRF_CAUA:Comstart
RF:LLRF_CAUA:Phincrate
RF:LLRF_CAUA:Pulses
RF:LLRF_CAUA:QuadSet
RF:LLRF_CAUA:Samples
RF:LLRF_CAUA:Stages
RF:LLRF_CAUA:UIncSet
RF:LLRF_Diag:Clock
RF:LLRF_Diag:Running
RF:LLRF_Loops:Clock
RF:LLRF_Loops:Running
RF:LLRF_fdlSourceA
RF:LLRF_fdlSourceB
RF:LLRF_fdlSourceA
RF:LLRF_fdlSourceB
epics>

```

Figure 7.8: LLRF PVs running on the Channel Access and listed after the execution of the *dbI* command on the EPICS prompt, VI

In the displayed PVs list, all diagnostics are also included, it means that the status of the system and its components can be now monitored using a proper interface or the suitable instructions on the command line. Database scanning for the LLRF diagnostics and readbacks PVs is determined to be periodic every second, besides, scanning mechanism supports hardware interrupts as well as software generated events, I/O event.

In order to test the I/O event mechanism and its latency time between a writing and its readback, a test on the *Cavity Voltage* parameter is shown in Fig. 7.9. *Cavity Voltage* parameter is used to set the desired power to the RF chain. This parameter has some transformations before the board can acquire it, thus, a long latency time is expected, more details on parameters transformation are shown in section 6.4.3.2. Latency time is defined here as the time from entering a new value through the interface to read it back on the



interface if and only if I/O event scanning is properly defined and the value has been correctly acquired by the FPGA board. The PV called RF:LLRF\_CAVA:Vset corresponds to the parameter that the operator can modify, that is the writing value, RF:LLRF\_CAVA:VRdbk corresponds to the readback value. Once the card has recognized the setting, acquired it, send it back to be transformed and showed on the interface as a readback, it can be presumed that all control system layers, showed in Fig. 6.4, have been crossed. Looking at Tab. 7.1, it can be concluded that the control system works on the scale of hundreds of microseconds and the scanning mechanism is performed in a negligible time. Other measurements of the latency time give similar results, small changes may be due to a further system load.

Table 7.1: *Cavity Voltage* parameter latency time

Latency Time		
Cavity Voltage set	Cavity Voltage readback	LT
50	49.99	62 $\mu$ s
100	100.01	49 $\mu$ s
150	150.00	57 $\mu$ s
200	199.99	50 $\mu$ s
250	250.00	61 $\mu$ s

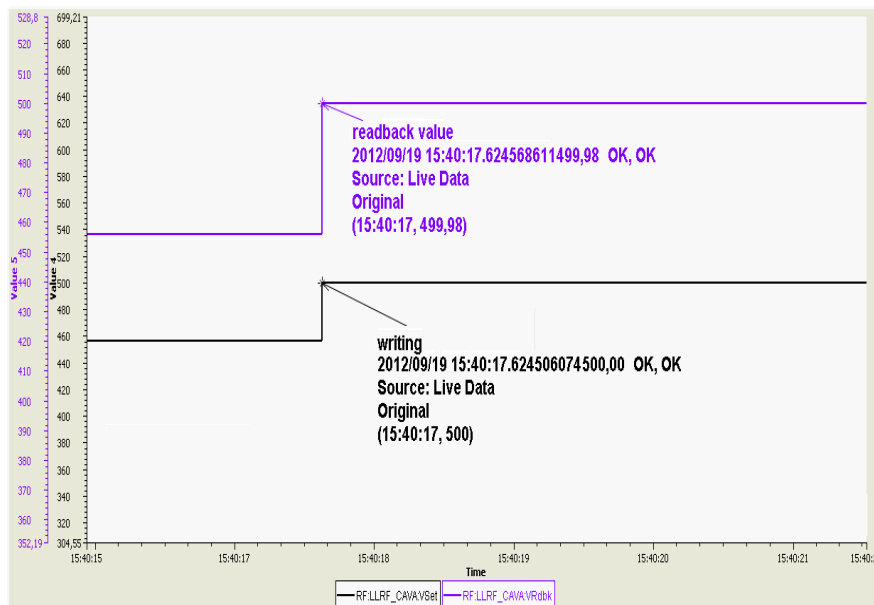


Figure 7.9: Latency time measured in *Cavity Voltage* set and readback

Finally, it is considered important to give some details of the appeared PVs in order to understand them and to certify the correct operation of the control system. Following the above criteria showed in the PVs lists in chapter 5, Tabs. 7.2, 7.4 and 7.3 incorporate the same information related to PVs:



- **Signal description:** Performance information of the signal.
- **Record type:** Type of record. Each record type has an associated set of record support routines depending on the record type. There are also some common properties to all records and some specific ones associated to some records types. These properties are referred to how monitors work, how scanning works, units data type, data precision, etc.
- **PV name:** Name of the process variable which runs through the Channel Access. This name must be unique to avoid collisions. It also must follow a naming convention to standardize the names circulating in the Channel Access.
- **EPICS device support:** Type of software support used to develop the control of the device to which the signal described corresponds. Device support takes care of the hardware specific details of record support.

Given the long list of PVs shown after the execution of the *dbI* command, the mentioned tables contemplate only the most representative PVs which are divided in three groups, main parameters in Tab. 7.2, main diagnostics in Tab. 7.4 and tuning and conditioning PVs in Tab. 7.3. Taking into account that each LLRF system controls two RF chains, PVs names can interchangeably have in their names *CAVA* for chain A or *CAVB* for chain B, its purpose and behavior is the same for both chains, for more details see 6.4.3.1.

Table 7.2: LLRF control system PVs description corresponding to main parameters

Parameter description	Record type	Process variable name	On Channel Access
Phase increase rate set	mbbo	RF:LLRF_CAVA:Phincrate	Yes
Phase shifter for ADCs	analog output	RF:LLRF_CAVA:Adcshift	Yes
Phase shifter for DACs	analog output	RF:LLRF_CAVB:Dacshift	Yes
Bit file version on Loops board	analog input	RF:LLRF_VersionRdbk	Yes
Send values to program VCXO	analog output	RF:LLRF_CAVA:Send	Yes
Enable beam pulsed mode operation	binary output	RF:LLRF_CAVB:Onpulse	Yes
Ki parameter readback for the PI loop	analog input	RF:LLRF_CAVA:kiRdbk	Yes
Number of samples to perform average	mbbo	RF:LLRF_CAVA:Samples	Yes
Cavity voltage amplitude readback	analog input	RF:LLRF_CAVA:CavampRdbk	Yes
Cavity voltage amplitude set	analog output	RF:LLRF_CAVA:CavampSet	Yes
Cavity phase amplitude readback	analog input	RF:LLRF_CAVA:CavphRdbk	Yes
Cavity phase amplitude set	analog output	RF:LLRF_CAVA:CavphSet	Yes
Amplitude reference minimum readback	analog input	RF:LLRF_CAVB:AmprefminRdbk	Yes
Amplitude reference minimum set	analog output	RF:LLRF_CAVA:AmprefminSet	Yes
Amplitude reference minimum readback	analog input	RF:LLRF_CAVA:AmprefminRdbk	Yes
Clock source set for Loops board	mbbo	RF:LLRF_Loops:Clock	Yes
When block is ON, parameters can't be written in the FPGA	analog input	RF:LLRF_blockParameters	Yes
Overwrite detection in dac1, Loops board	analog input	RF:LLRF_Loops:Over1	Yes
Set all gain dac values as the value written in gain 1	analog output	RF:LLRF_CAVA:Gain1L	Yes
Start Loops board running state. Acquisition ON	analog output	RF:LLRF_Loops:Running	Yes

Table 7.3: LLRF control system PVs description corresponding to tuning and conditioning parameters

Parameter description	Record type	Process variable name	On Channel Access
Automatic tuning enable in MEBT	binary output	RF:LLRF_CAVA:OnTuning	Yes
Set number of steps for the motor controller in MEBT tuning	analog output	RF:LLRF_CAVB:Numsteps	Yes
Enable the move of the plunger in MEBT tuning	binary output	RF:LLRF_CAVA:OnMovePlg	Yes
Enable frequency tuning mode for RFQ cavities tuning	binary output	RF:LLRF_CAVA:CAVB:OnFreqTun	Yes
Enable tuning reset motor controller in MEBT tuning to move the plunger a number of pulses defined by pulses	binary output	RF:LLRF_CAVA:OnTunreset	Yes
Choose the frequency of the pulses for the movement of the motor in MEBT tuning	mbbo	RF:LLRF_CAVA:Pulses	Yes
Set margin up dead-band. If tuning dephase is above this margin the plunger will be moved	analog output	RF:LLRF_CAVA:Marginup	Yes
Set margin up dead-band. If tuning dephase is below this margin the plunger will be moved	analog output	RF:LLRF_CAVA:Marginlow	Yes
Enable the manual tuning mode to test the tuning loop in MEBT	binary output	RF:LLRF_CAVA:Plgmanual	Yes
Enable RF drive pulse modulated for conditioning	binary output	RF:LLRF_CAVA:OnPulsMode	Yes
Set the duty cycle of the pulses for conditioning	analog output	RF:LLRF_CAVA:DCycleSet	Yes
Enable the information about the vacuum state of the cavity	binary output	RF:LLRF_CAVA:OnVacIlk	Yes

Table 7.4: LLRF control system PVs description corresponding to main system diagnostics

Parameter description	Record type	Process variable name	On Channel Access
Amplitude readback of the cavity volt RF signal	analog input	RF:LLRF_CAVA:AVolRdbk	Yes
Phase readback of the cavity volt B RF signal	analog input	RF:LLRF_CAVB:PhasVolRdbk	Yes
Amplitude proportional error readback for PI loop	analog input	RF:LLRF_CAVB:AErrPropRdbk	Yes
Cavity voltage reference adjust readback, applied for calibration	analog input	RF:LLRF_CAVA:refadjustRdbk	Yes
End T1 readback for beam pulsed mode	analog input	RF:LLRF_CAVA:Aendt1Rdbk	Yes
I component readback for reference cavity RF signal	analog input	RF:LLRF_CAVA:IRefRdbk	Yes
Q component readback for reference cavity RF signal	analog input	RF:LLRF_CAVB:QRefRdbk	Yes
Amplitude readback of the forward cavity RF signal	analog input	RF:LLRF_CAVA:AfwVolRdbk	Yes
Phase readback of the reverse power RF signal	analog input	RF:LLRF_CAVA:PhasrvVolRdbk	Yes
Amplitude readback of the reverse RF power in the circulator	analog input	RF:LLRF_CAVA:ArvCircRdbk	Yes
Phase readback of the reverse RF power in the circulator	analog input	RF:LLRF_CAVB:ArvCircRdbk	Yes
I component readback of the amplitude forward RF signal in the amplifier 1	analog input	RF:LLRF_CAVA:Ifw1AmpRdbk	Yes
Q component readback of the amplitude forward RF signal in the amplifier 2	analog input	RF:LLRF_CAVA:Qfw2AmpRdbk	Yes
Amplitude readback of the reverse RF power in the amplifier 2	analog input	RF:LLRF_CAVA:Arv2AmpRdbk	Yes
Phase readback of the tuning dephase signal	analog input	RF:LLRF_CAVA:TunDPhaseRdbk	Yes
Plunger moving up readback for MEBT motor controller	analog input	RF:LLRF_CAVB:Plgup	Yes

### 7.2.1.2 Interlock PVs test

As it has been mentioned in multiple occasions throughout this work, the interlock system is a fundamental part for the proper functioning of LIPAc. In sections 6.4.4.9 and 6.4.5, it is detailed how LLRF system manages and interfaces several groups of interlocks (arcs, vacuum and multipacting) coming from RFQ, MEBT and SRF Linac, but obviously, these interlocks can not be simulated in this test-bench. For that purpose is the manual interlock, which simulates the behavior of the control system in the same manner as if it were a real interlock. Control system interface area where parameters used for interlock detection are displayed can be seen in Fig. 7.10.

The response time for the interlock PVs test is showed in Fig 7.11, where is possible to observe the sequence of activation of the readbacks and their latency time employee in read/write to/from the Channel Access. The execution of the test is as follows:

1. Annotation 1 corresponds to the activation of the manual interlock for the pretended MEBT cavity, an action carried out by the operator pressing the appropriate boolean button which sends a 1 to the EPICS Channel Access by means of a PV called *RF:LLRF\_CAVA:OnllkManual*, this action simulates the arrival of an external interlock regardless of the kind.
2. Once the manual interlock have been activated, three actions happen. First one corresponds to annotation 4, a diagnostic PV called *RF:LLRF\_CAVA:FimdelayRdbk* that reads back a 1 from the Channel Access, it occurs 218 ms after the arrival of the supposed external interlock, the corresponding boolean button state changes from OFF to ON in the LLRF control interface. This action is achieved in the range of milliseconds. As it can be seen below, the rest of the status PVs arrived almost at the same time after the *RF:LLRF\_CAVA:FimdelayRdbk* activation. That means the device driver takes millisecond to respond for the first time because it is developing several parallel operations related to the interlock identification and diagnosis.
3. The second action happens in the interlock module part and indicates to the operator what kind of interlock has happened, this action is registered  $7\mu\text{sec}$  after the first alert. It corresponds with the annotation 2, and reads back a value of 256, the associated diagnostics PV is called *RF:LLRF\_CAVA:FidTotal*. As explained in section 6.4.4.9, the interlock output module is a byte based widget, manual interlock corresponds with the bit located in the ninth position, that is  $2^8 = 256$ . This byte based solution increases the response speed of the system.
4. Last action takes place again only  $6\mu\text{sec}$  later, it corresponds with the annotation 3, reading 63 from the Channel Access, this output is byte based as well, and means how many actions of the output list are carried out after an interlock alarm, the diagnostic PV is called *RF:LLRF\_CAVA:llkDiagDAC* and is composed by 6 bits, if all of them are equal to 1, then 63 is the readback, that is, all possible actions have been achieved.

Although response times of interlock PVs range from milliseconds to microseconds and they can be considered low response times, it is important to note that the RF emergency stop is autonomous of these PVs performance, that is, independent of EPICS. RF power

emergency stop does not follow any EPICS software process, do not operate using the EPICS Channel Access. In any case, it is believed essential to warn the operator in real time by the pertinent alarms and diagnostics, once the machine has been secured. The fulfillment of that warning is what this test has characterized.

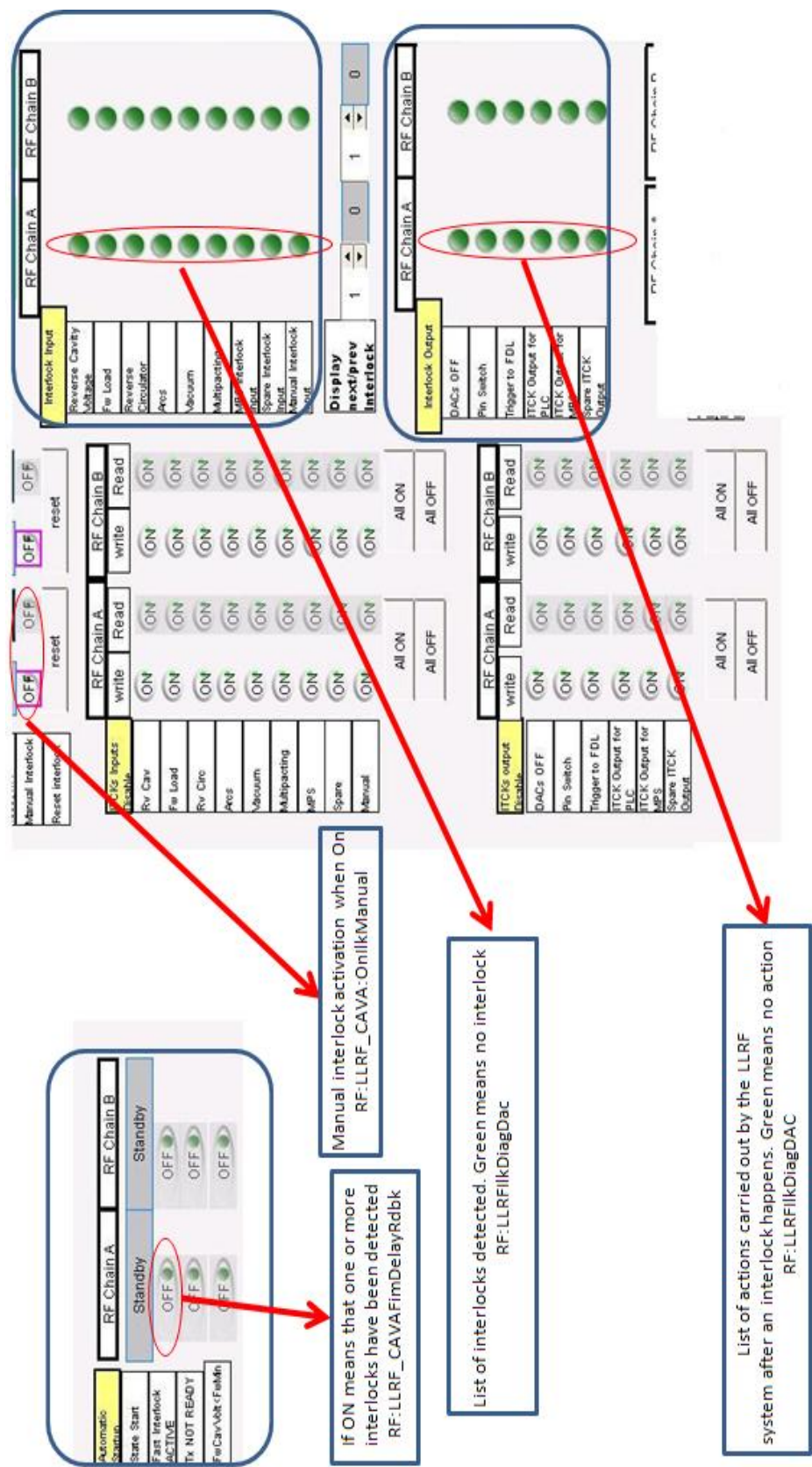


Figure 7.10: Parameters used for the interlock detection and diagnosis displayed in the LLRF control system GUI

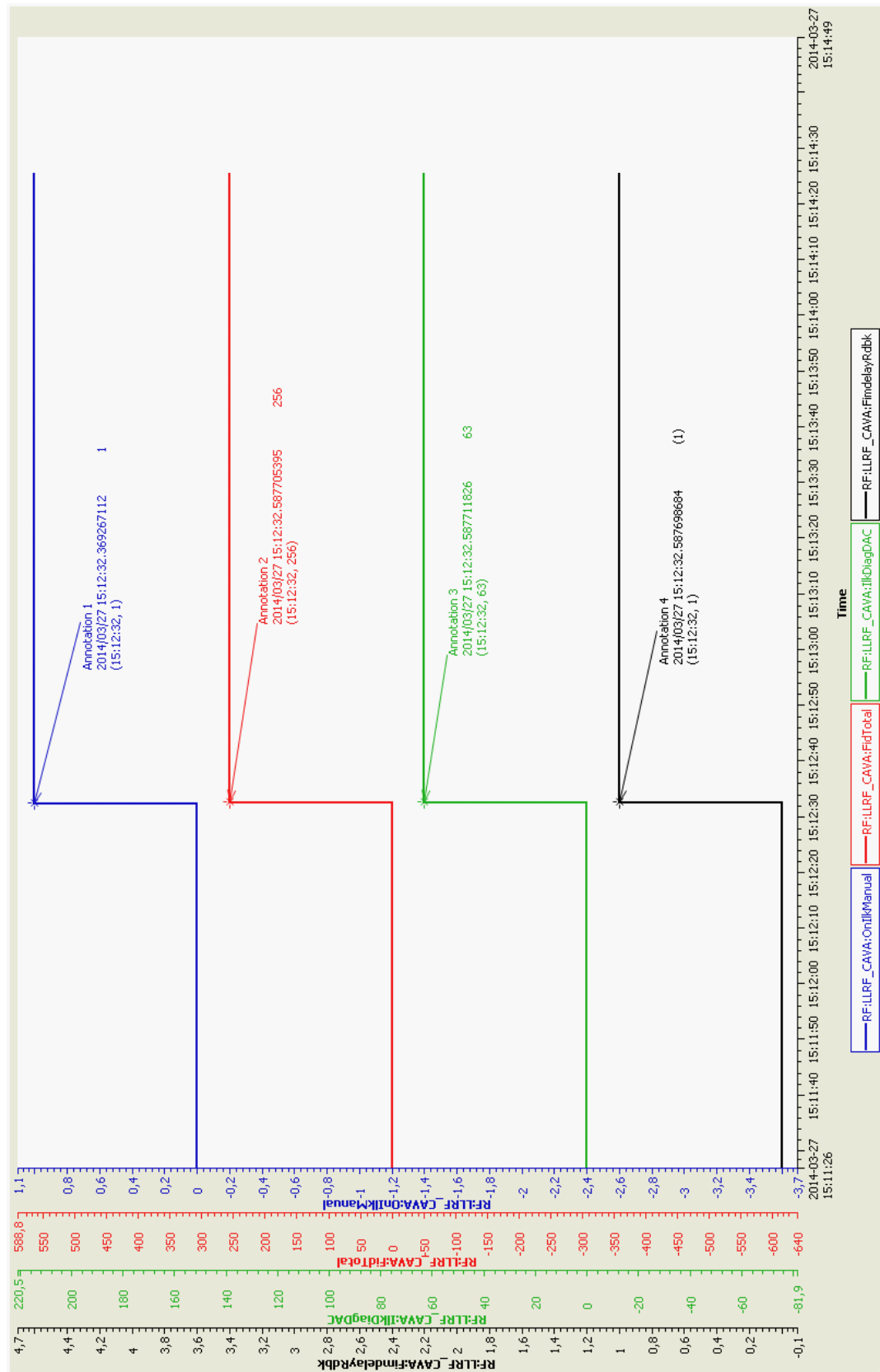


Figure 7.11: Latency time measured in the interlock PVs test



### 7.2.1.3 Gain PVs test

Lyrtech cards have variable gain amplifiers in the analogue inputs and outputs in DACs and ADCs. Gain values are modifiable through the system interface. One of the most relevant characteristic that the gain control supports is the possibility of setting all channels gain values like the value of the first channel. This option is very useful if ADCs are being overrun and it is mandatory to decrease their values as fast as possible in order to avoid important damage. With this choice, the operator only needs to change the value of the channel 1 and press a button to have the same gain in the rest of the channels.

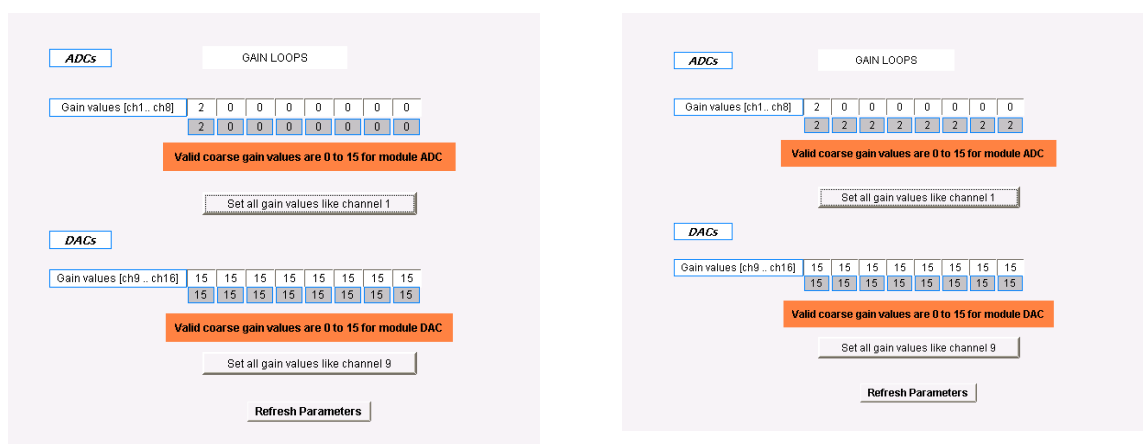


Figure 7.12: Gain values are set equal to channel 1

Gain test starts from a hypothetical situation in which ADCs are experiencing an overrun alarm that requires to modify all the ADCs values as soon as possible. The fastest way to do it is just changing the value in the first channel and transmit that value to the rest of channels, instead of writing each value manually. Gain interface showing the explained situation can be seen in Fig. 7.12. First, only ADC channel 1 is equal to 2, the rest are 0, second, all ADCs values are equal to channel 1 without writing any value in the interface, just pressing *Set all values like channel 1*. In order to set all gain values like channel 1, the device driver writes twice in the same offset <sup>1</sup> but in different groups of bits, one group of four bits for each channel, bits scheme for the below offsets is showed in Fig. 7.13. The advantage of this development is when programming at such low level, the data processing speed is extremely high as shown in the test displayed in Fig. 7.14 and executed as follows:

1. Annotation 15 corresponds with readback of the channel 1, it is the channel that has been manually changed.
2. Annotation 8 to annotation 14 are the readbacks of the channels 2, 3, 4, 5, 6, 7 and 8 after pressing the button *Set all values like channel 1*.
3. Pressing *Set all values like channel 1* button triggers the first readback corresponding to channel 2 with a PV called `RF:LLRF_CAVA:Gain2Rdbk`, it appears in the EPICS

<sup>1</sup>FPGA register address given in hexadecimal code. Gain offsets for gain writing are: 0x0028 for channels 1 and 2, 0x002C for channels 3 and 4, 0x0030 for channels 5 and 6 and 0x0034 for channels 7 and 8

Channel Access at *16:51:19.132821029* and the last readback corresponding to channel 8 with a PV called *RF:LLRF\_CAVA:Gain8Rdbk* appears  $138\mu s$  later. The control system has passed through all layers to reach the offsets, it has modified all gain values and it has come back to the EPICS device support to send the values to the Channel Access, again, in the hundreds microseconds range.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												Channel (N+1) programmable gain value			
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												Channel N programmable gain value			
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Figure 7.13: Bit scheme for the programmable ADCs gain

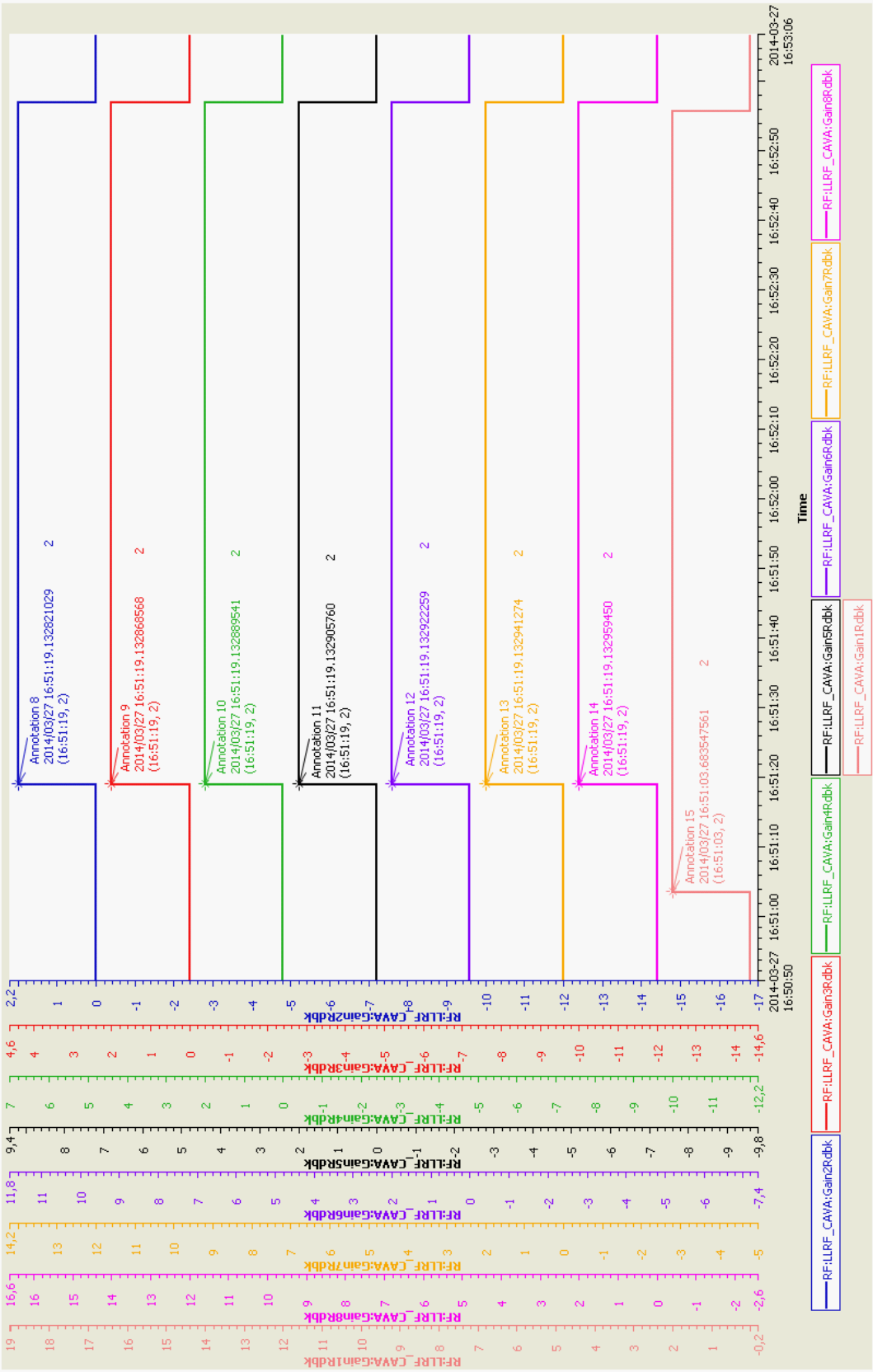


Figure 7.14: Latency time measured in the gain PVs test

#### 7.2.1.4 MEBT tuning PVs test

One of the more relevant tasks of the LLRF system is to carry out the tuning of the MEBT buncher cavity. The tuning is used to keep the resonance frequency of the cavity equal to the master oscillator frequency. For doing so, a plunger is moved in and out of the cavity body in order to change its geometry and adjust any deformation due to thermal drifts. As explained in section 6.4.5, LLRF manages the mechanical tuning of the MEBT, using a plunger which is moved with a stepper motor. Through the LLRF control system interface, the operator can configure this tuning in manual or automatic mode. Parameters and interface areas used for tuning are showed in Fig. 7.15.

Following test, Fig. 7.16, illustrates a hypothetical case where it is necessary to configure the manual tuning and to define some parameters associated to the motor movement, control system interface reacts showing the proper readbacks and carrying out the precise options. Manual tuning must be used at very low power and preferably the first time the cavities are powered up. Due to the amount of information in this test, marked annotations are explained separately:

- Annotation 1 and 10. Both belong to a PV called *RF:LLRF\_CAVA:Numsteps*. It defines the number of steps that the stepper motor should execute. This PV is represented twice in order to have a better time comparative perspective both above and below of the figure.
- Annotation 2 and 9. Both belong to a PV called *RF:LLRF\_CAVA:NumstepsRdbk*. It shows the readback value of the number of steps once it has been properly written in the Loops board. This PV is represented twice in order to have a better time comparative perspective both above and below of the figure.
- Annotation 3. It corresponds to a PV called *RF:LLRF\_CAVA:Pulses*. It sets the frequency of the pulses for the stepper motor. Definable frequencies are a predefined list, to do this, this PV is a multi bit binary output, each frequency value corresponds to a different parameter that only FPGA board can understand, nevertheless the corresponding frequency values can be understood by the operator.
- Annotation 4. It corresponds to a PV called *RF:LLRF\_CAVA:PulsesRdbk*. It shows the readback value of the frequency of the pulses for the stepper motor once it has been properly written in the Loops board.
- Annotation 5. It corresponds to a PV called *RF:LLRF\_CAVA:OnTuning*. It sets the plunger ON.
- Annotation 6. It corresponds to a PV called *RF:LLRF\_CAVA:OnTuningRdbk*. It shows the readback value of the activation state of the tuning. If it is ON means this value has been properly written and the motor configuration parameters are sent to the motor controller, the plunger movement is enable, tuning begins.
- Annotation 7. It corresponds to a PV called *RF:LLRF\_CAVA:PlgmanRdbk*. This PV corresponds to a tuning diagnostic that indicates ON when the plunger is behaving in the manual mode. Automatic mode must remain disable.

- Annotation 8. It corresponds to a PV called *RF:LLRF\_CAVA:PlgupRdbk*. This PV corresponds to a tuning diagnostic that shows the direction of movement of the plunger, if this readback is ON means the plunger is moving up.

In Fig. 7.16 number of steps are set to 1000, annotation 1; the frequency of the motor pulses are set to 250Hz, annotation 3; then the plunger movement is ON, annotation 6; 265 $\mu$ s later the control system reacts and indicates that the plunger is going to move in manual mode in upward direction, annotations 7 and 8, the motor movement begins. Once the number of steps have been achieved by the motor, the move stops and the up movement PV changes to 0 to mean the plunger is stopped, annotation 8.

One more example of the plunger movement can be seen in Fig. 7.17. In this example the order of the annotations represent the same PVs as before, 11 is the same as 1, 2 as 12 and so on. Unlike the previous example, the configuration parameters are not 0 as initial values. This test shows an hypothetical situation where the control system must execute the actions even when the parameters change dynamically and the system is not coming from the initial state. As can be seen, the plunger was moving with a given configuration but suddenly the operator decides to change some parameters. Number of steps changes from 500 to 800 and the frequency pulses go from 500Hz to 250Hz. Accordingly, tuning move PV, annotation 15, changes from ON to OFF and again to ON, then, new configuration is taken into account and the movement is executed properly 84 $\mu$ s after. The duration of the movement, that can be seen in annotation 18, is shorter, in comparison with the previous test, due to the plunger was moving before, not from the initial state, part of the movement was achieved with the previous configuration and the number of pulses to achieve in this situation is smaller.

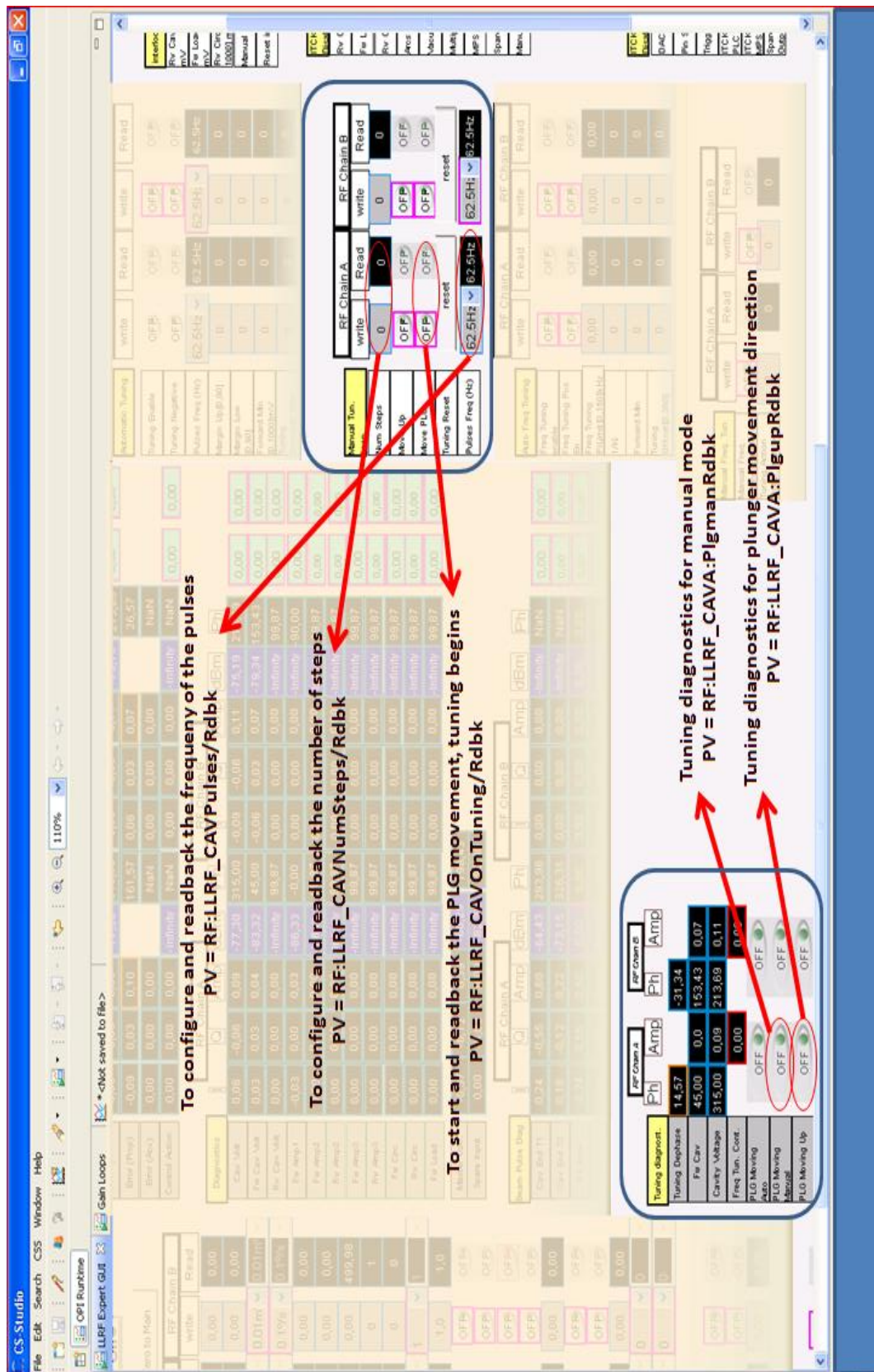


Figure 7.15: Parameters for MEBT tuning in the LLRF control system interface

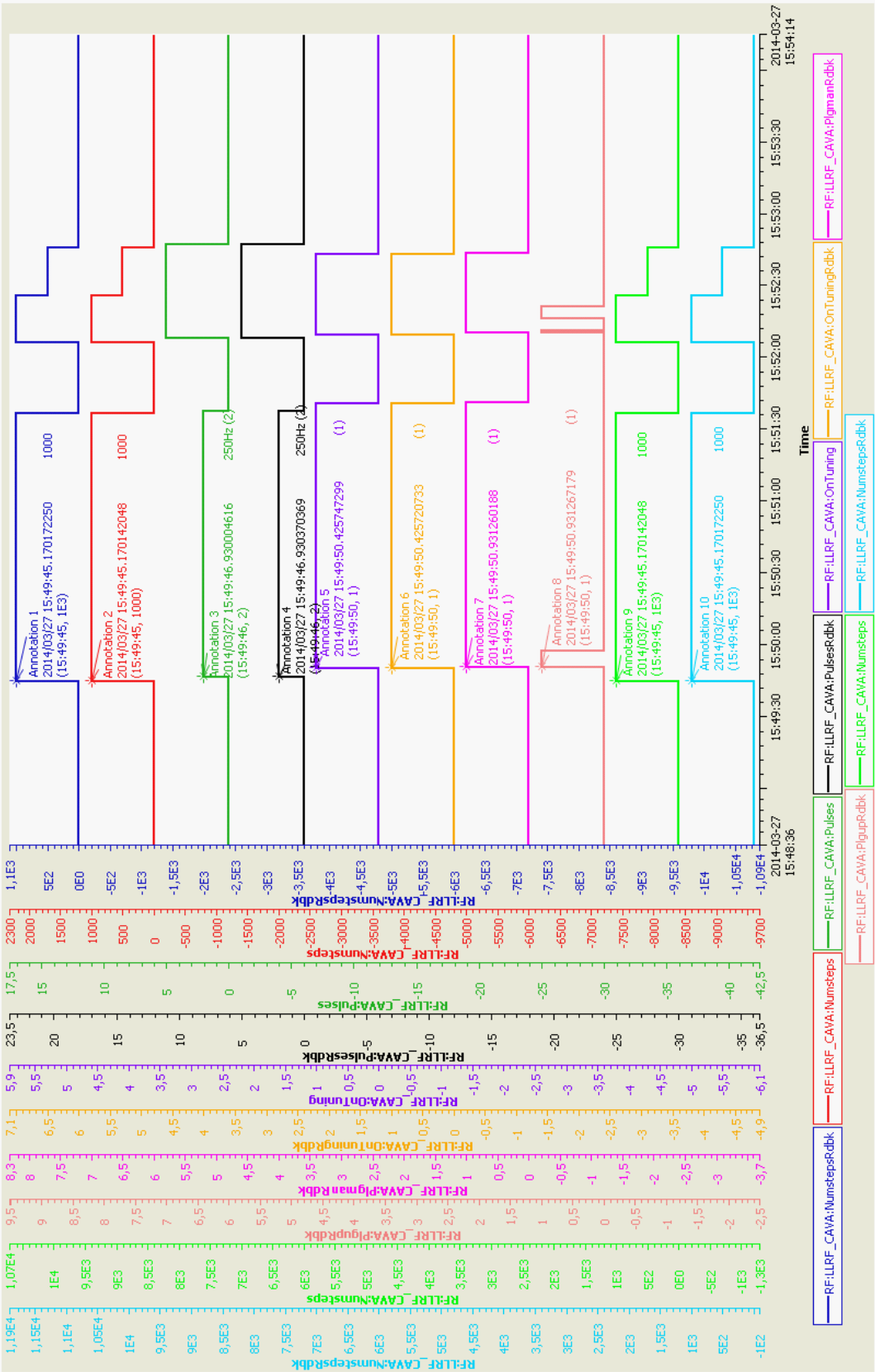


Figure 7.16: Latency time measured on the MEBT tuning PVs test I

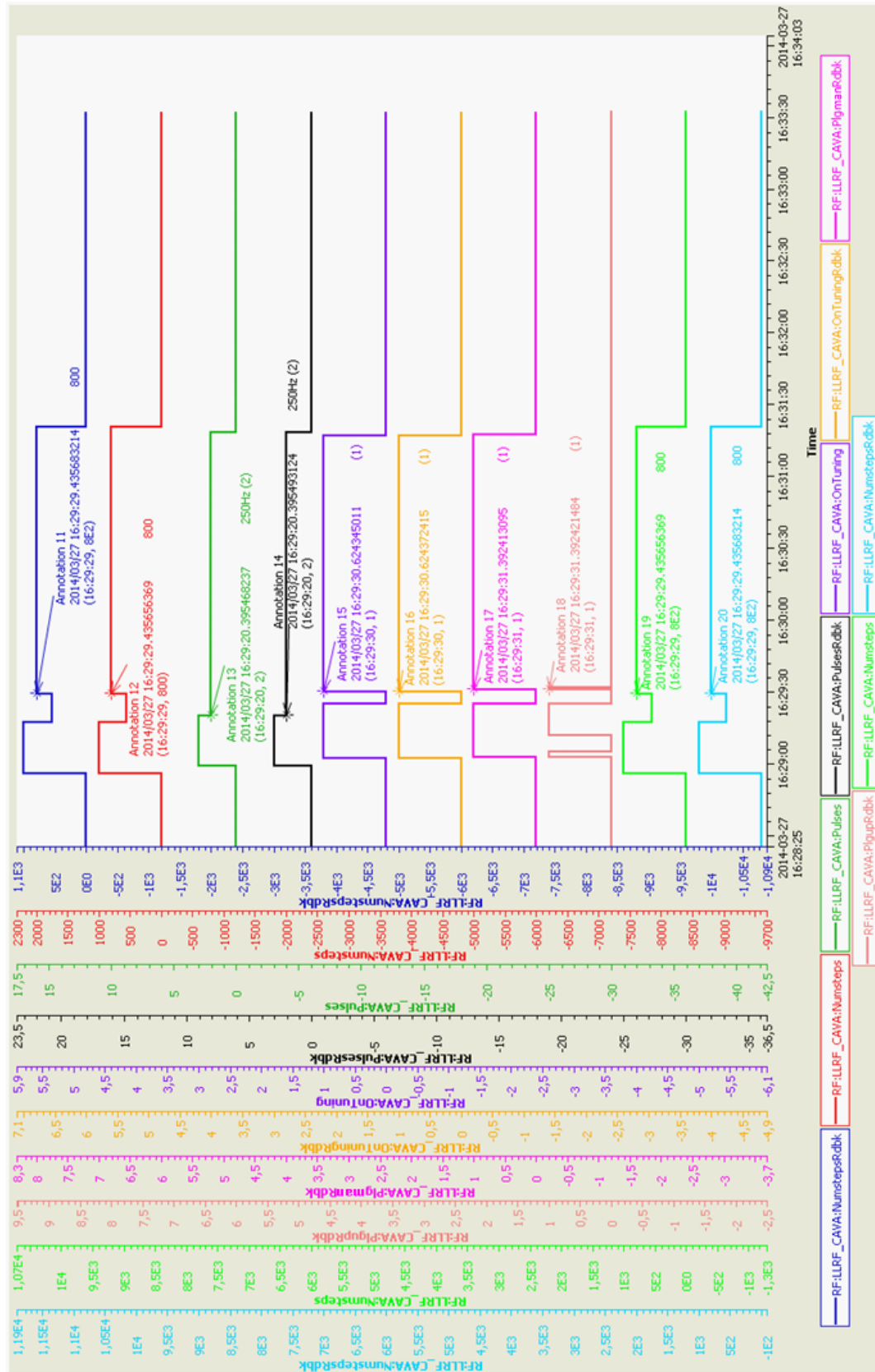


Figure 7.17: Latency time measured on the MEBT tuning PVs test II



## 7.2.2 Amplitude and phase loop tests

Once the communication between control system layers have been tested and the PVs behavior have been studied, following tests simulate the supply of power to the RF chains. This hypothetical operation would be executed in the same manner no matter if the cavities belong to MEBT, SRF Linac or RFQ subsystem. PVs details are not given anymore in following sections but a global view of the operation is explained, where the control system plays a fundamental role one more time.

Following tests are related to the amplitude and phase loop behavior. It is important to bear in mind that the main goal of these tests is not the output of the system, i.e., RF signal shape, RF signal amplitude or phase values, but the role of the control system to properly allow the operator to reproduce actual situations in different modes of operation. To generate a 175 MHz RF signal with real-time variable amplitude and phase in order to feed the RF chains and to digitize the RF signal for diagnostics are the basic functions of the LLRF system. Following tests are focused on these procedures both in open/closed loop and in continuous/pulsed mode, detailed in sections [7.2.2.1](#), [7.2.2.2](#), [7.2.2.3](#) and [7.2.2.4](#).

### 7.2.2.1 Test on continuous wave and open loop

In this test, a basic RF signal generation is shown. To generate a RF signal, at least amplitude signal and phase signal must be specified using the control system interface, the LLRF control system allows the operator to modify these parameters in real-time. In order to make the FPGA board understand these parameters, a coordinates transformation, explained in section [6.4.3.2](#), is performed.

In Fig. [7.18](#), a part of the LLRF control system interface is exposed. The image shows the state of the LLRF system in a certain moment. Looking at Main Parameters area, two parameters can be seen, *Cavity Voltage*, which specifies the amplitude of the RF signal and *Cavity Phase*, that specifies its phase, first one is now 80mv and second one is 0 degrees, both are only defined for chain A.

In the Main Diagnostics area, under the *AmpPhase* label, five diagnostics can be seen. Each diagnostic is composed by various parameters: I component of the RF signal, Q component of the RF signal, amplitude in mV, amplitude in dBm and phase of the RF signal. *Cavity Ref* and *Cavity Volt* represent the diagnostics of the RF signal in different points of LLRF system, *Cavity Ref* is measured at the input of the LOFE and *Cavity Volt* is measured at the output of the LOFE. *Cavity Ref*, as its own name says, is used as a reference, that is the RF signal that the operator wants to have at the output of the LOFE. In Fig. [7.19](#) the points where the diagnostics are measured can be observed, LOFE module executes a frequency transformation on the RF signal, from 25 Mhz (signal generated by the FPGA) to 175 Mhz (system work frequency), thus, different values on both diagnostics are expected due to the attenuation of the change in frequency. *Cavity Ref* will always be an equivalent value to that introduced by the operator but with slight variations due to the transformations carried out by the control system, more details are given in [6.4.3.2](#). Therefore, entering 80mv of amplitude signal in the *Cavity Voltage*, gives a readback value of 80.11 mV in the amplitude (Amp) of *Cavity Ref* and a readback of 59.15 mV in the amplitude (Amp) of *Cavity Volt*. *Control Action* diagnostic corresponds to the action carried out by the PI loop

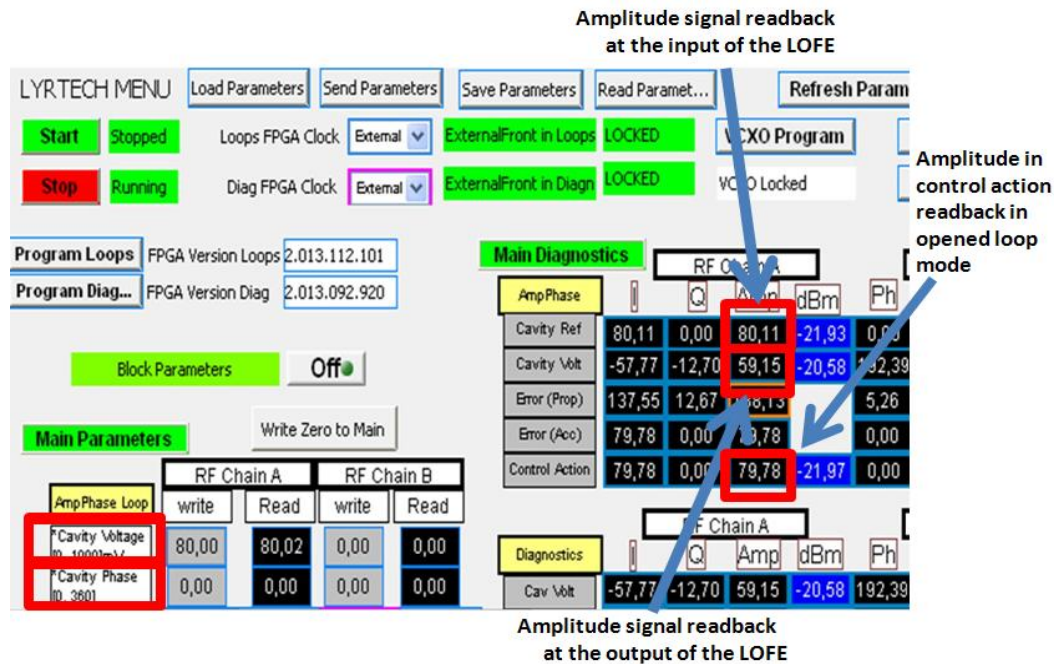


Figure 7.18: Image of the LLRF control system GUI taken during a test configured in open loop mode. Some values of main parameters and main diagnostics can be observed

to correct the difference between *Cavity Ref* and *Cavity Volt* but as it can be seen in 7.18, *Control Action* Amp readback is almost equal to 80 mV, the same value as the reference, that means no action is being performed cause the system is working in **open loop mode**, which is the default mode of the system.

As a result of the configuration detailed above, a 175 MHz RF signal at the output of the loops front end (LOFE), can be seen in 7.20, this figure corresponds to the view of the RF signal on an oscilloscope. The LLRF control system is, thus, able to communicate with the FPGA and to send the correct values and do the right transformations in order to create a RF signal.

In Tab. 7.5, the relation between amplitude writings values in *Cavity Voltage* and read-backs of the amplitude (Amp) component in *Cavity Ref*, *Cavity Volt* and *Control Action* diagnostics is shown, with the system working in open loop mode and continuous wave. *Cavity Voltage*, *Cavity Ref* and *Control Action* take mostly common values in all measurements as shown in Fig. 7.21, caused by the open loop operation. *Cavity Volt* value is always lower than the others due to the amplitude attenuation resulting from the frequency transformation.

#### 7.2.2.2 Test on continuous wave and closed loop

In this section a test in closed loop mode is presented. Closing the loop is a complex operation that must be carried out with utmost care, the system has to be powered up slowly in order to

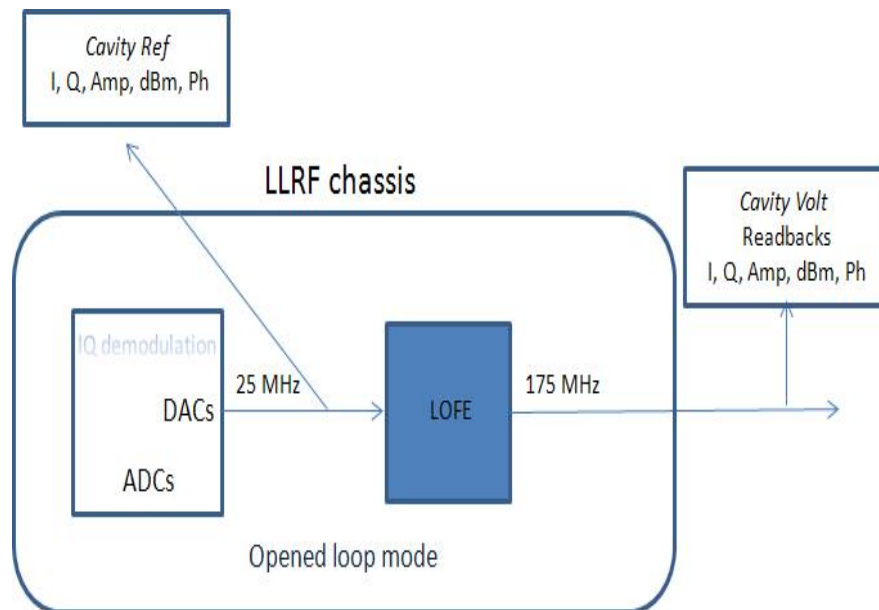


Figure 7.19: System scheme in open loop showing the reference and the readback at the output. LOFE executes a frequency change and the amplitude of the signal decreases

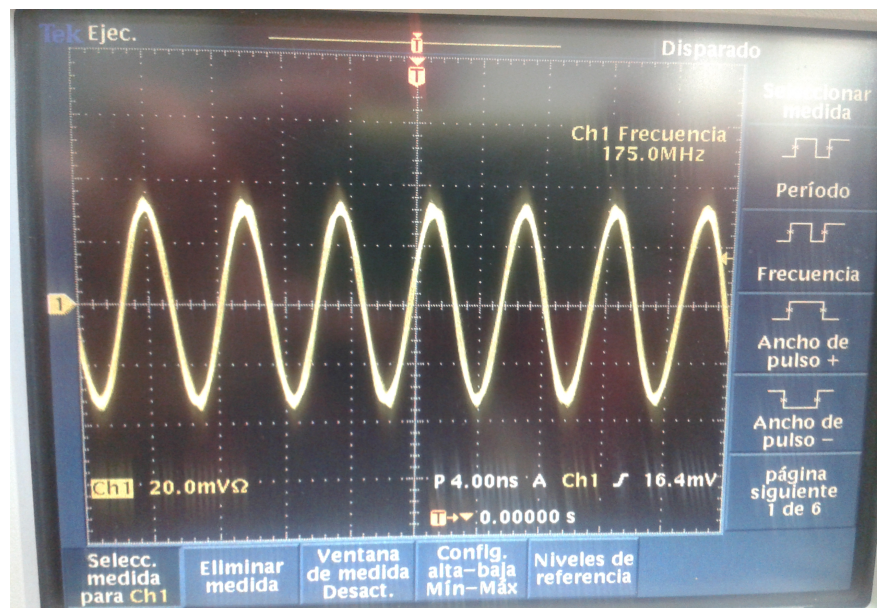


Figure 7.20: Image of a 175 MHz RF signal measured at the output of the LOFE

avoid damage and to check that the control system is correctly interpreting the data entered by the operator.

Closing the amplitude and phase loop means that if the operator wants to have  $X$  mV in the cavity, as amplitude signal, and  $Y$  degrees, as phase signal, the loop has to ensure that there are always those values, irrespective of the attenuation encountered by the RF

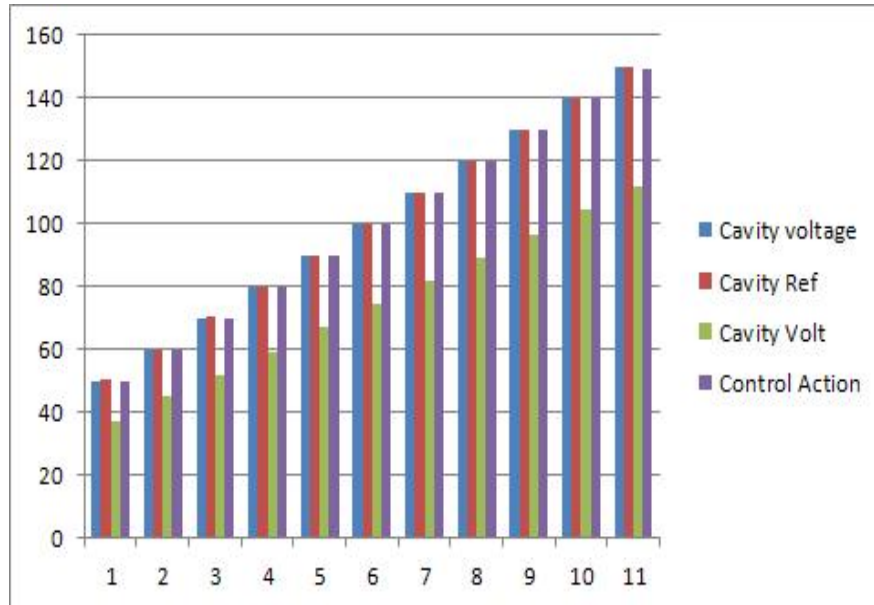


Figure 7.21: Diagram showing the evolution of measurements displayed in Tab. 7.5, as a function of *Cavity Voltage* value entered by the operator. *Control Action* has the same value as *Cavity Voltage*, no proportional gain is applied in open loop mode

signal. If there are disturbances in the system that, for example, decrease the amplitude, the loop compensates this changes in real time, trying to accomplish initial values required by the operator. In the present test, closing the loop is necessary to have the same readbacks of the signal both at the entry and at the output of the LOFE, an schematic view of the system where position the diagnostics *Cavity Ref* and *Cavity Volt* are located, is shown in Fig. 7.22.

A PI loop<sup>2</sup> is applied to the I&Q components of the *Cavity Voltage* signal. The behaviour of the PI loop is defined at FPGA level and it is out of the target of this work, but the reference point and parameters of the loop are adjustable through the control system interface in order to make the response of the loop faster or slower (proportional-constant= $K_p$ , integral-constant= $K_i$ ). Besides the PI loop configuration parameters, there is a boolean button, see Fig. 7.23, which enables or disables the closed loop mode by means of sending 0 (OFF) or 1 (ON) to the Channel Access using a binary record type. An example of the LLRF control interface status after enabling the closed loop mode can be seen in Fig. 7.24.

Tab. 7.6 shows data taken in closed loop working mode. It can be observed a relation between the initial amplitude entered by the operator, *Cavity Voltage*, and its diagnostics, in closed loop mode. As can be seen, *Control Action* is taking proportional values to increase the amplitude in *cavity Volt* until it is equal to *Cavity Voltage*. *Control Action* takes larger values, with the same input, than in open loop, it represents a proportional gain applied to

<sup>2</sup>A proportional-integral-derivative controller (PID controller) is a generic control loop feedback mechanism (controller) widely used in industrial control systems. A PID controller calculates an *error* value as the difference between a measured process variable and a desired setpoint. The controller attempts to minimize the error by adjusting the process control inputs. A PI Controller (proportional-integral controller) is a special case of the PID controller in which the derivative (D) of the error is not used.

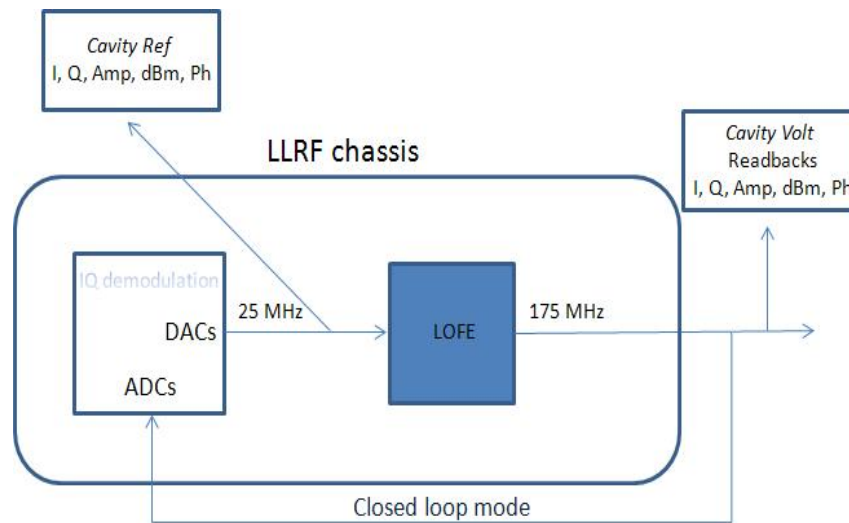


Figure 7.22: System scheme in closed loop showing the reference and the readback at the output. LOFE executes a frequency change and the amplitude of the signal decreases but it is compensated by the PI loop through *Control Action* parameter



Figure 7.23: Image of button to enable or disable the closed loop mode in the LLRF control system GUI. If it is ON the system operates in closed loop mode

the amplitude component of the signal as a result of the PI loop operation. In the diagram shown in Fig. 7.25 it can be observed that the values are growing proportionally and the system have the same value both at the input of the LOFE, *Cavity Ref*, and at the output of the LOFE, *Cavity Volt*, despite the disturbance occasioned by the frequency transformation.

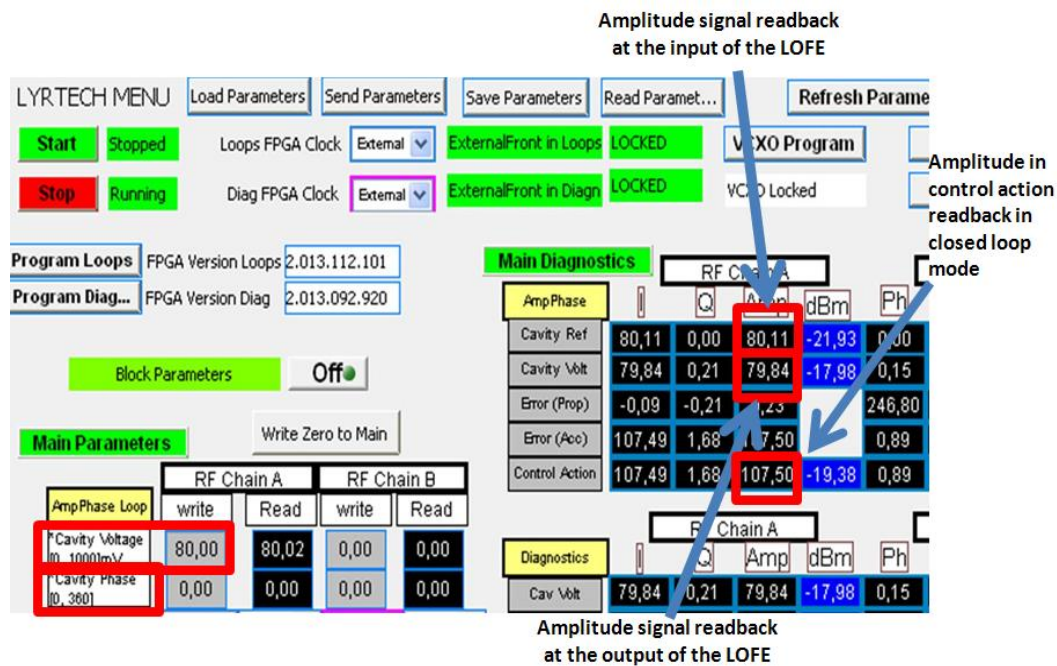


Figure 7.24: Image of the LLRF control system GUI taken during a test configured in closed loop mode. Some values of main parameters and main diagnostics can be observed

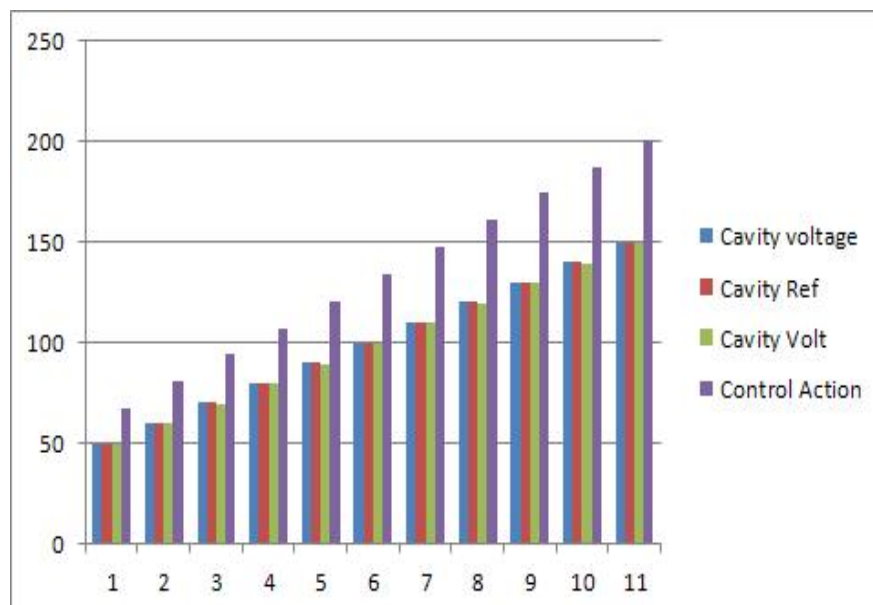


Figure 7.25: Diagram showing the evolution of measurements displayed in Tab. 7.6, as a function of *Cavity Voltage* value entered by the operator. *Control Action* is always the biggest value to compensate the disturbance of the system. The initial value and its readbacks are equally growing

Table 7.5: Data taken in continuous wave and open loop mode as a function of the values entered by the operator in *Cavity Voltage*

Cavity Voltage	Cavity Volt	Control Action
50	37.38	49.9
60	44.84	59.58
70	51.52	69.89
80	59.12	79.78
90	67.08	89.75
100	74.24	99.67
110	81.75	109.59
120	89.27	119.6
130	96.7	129.58
140	104.21	139.59
150	111.67	149.48

Table 7.6: Data taken in continuous wave and closed loop mode as a function of the values entered by the operator in *Cavity Voltage*

Cavity Voltage	Cavity Volt	Control Action
50	49.9	67.46
60	59.86	80.82
70	69.89	94.1
80	79.81	107.48
90	89.75	121
100	99.65	133.97
110	109.65	147.5
120	119.6	160.99
130	129.58	174.51
140	139.59	187.75
150	149.48	201.16

### 7.2.2.3 Test on pulsed mode and open loop

As explained in previous chapters, LIPAc has two operating modes, continuous wave and pulsed mode, see section 5.10.1. In the GUI of LLRF control system, the pulsed mode operation is managed by a combination of pulse activation and pulse width. In Fig. 7.26, the interface area where the pulse mode can be configured, is shown.

Conditioning	RF Chain A		RF Chain B	
	write	Read	write	Read
Pulse Mode	ON	ON	OFF	OFF
Vacuum interlocks	OFF	OFF	OFF	OFF
Pulse width [0,100 ms]	50	50	0	0
AmpRefMin [0,1000] mV	0,00	0,00	0,00	0,00
Cavity Voltage [0,1000] mV	80,00	80,02	0,00	0,00

Figure 7.26: Image of the LLRF control system GUI where the pulsed mode is presented. Pulse mode and pulse width must be modified

To achieve this test, an hypothetical pulsed operation is configured. *Pulse Width* is defined with 50ms, taking into account that the maximum period of the signal is 100ms and then, *Pulse Mode* parameter is set to ON. *Cavity Voltage* takes the same value as before, 80mV. The RF signal generated in pulsed mode is showed in Fig. 7.27. It can be observed that the pulse occupies half the period, thus, *Pulse Width* and *Pulse Mode* parameters have properly received and sent the information by means of the control system.

### 7.2.2.4 Test on pulsed mode and closed loop

In this test, the system remains in pulsed mode but the loop is closed, the length of the pulse is configured at the half of the maximum, as in the previous test, 50ms.

Looking at Fig. 7.28 a similar signal as before can be observed. The unique difference is that the signal takes an undetermined time to reach the final value because the PI loop need a convergence time in each pulse. This test demonstrates the ability of the parameters of the control system to work together, combining different working modes at the same time, pulsed mode, closed loop and PI loop configuration parameters.



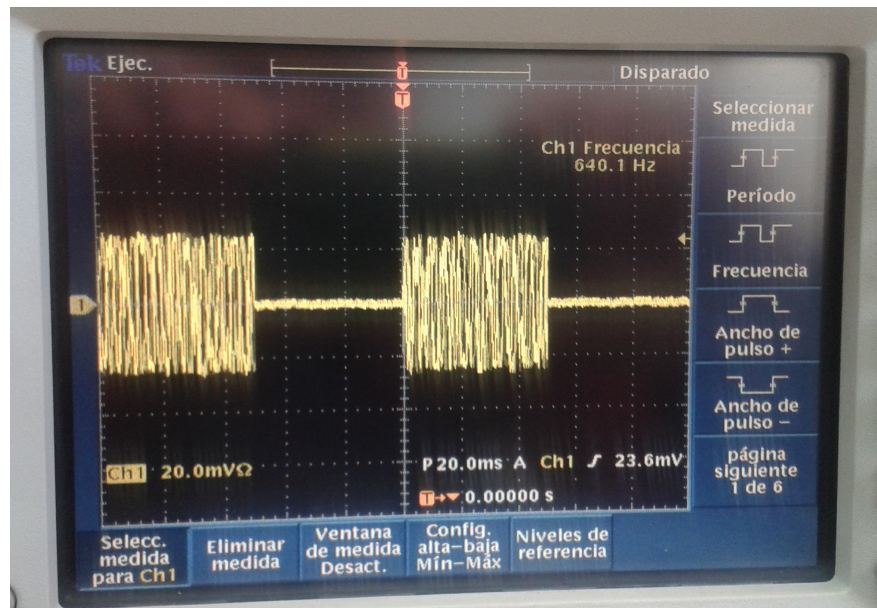


Figure 7.27: Image of RF signal generated in pulsed mode and open loop. Pulse duration is 50 ms, which corresponds with the half of the period

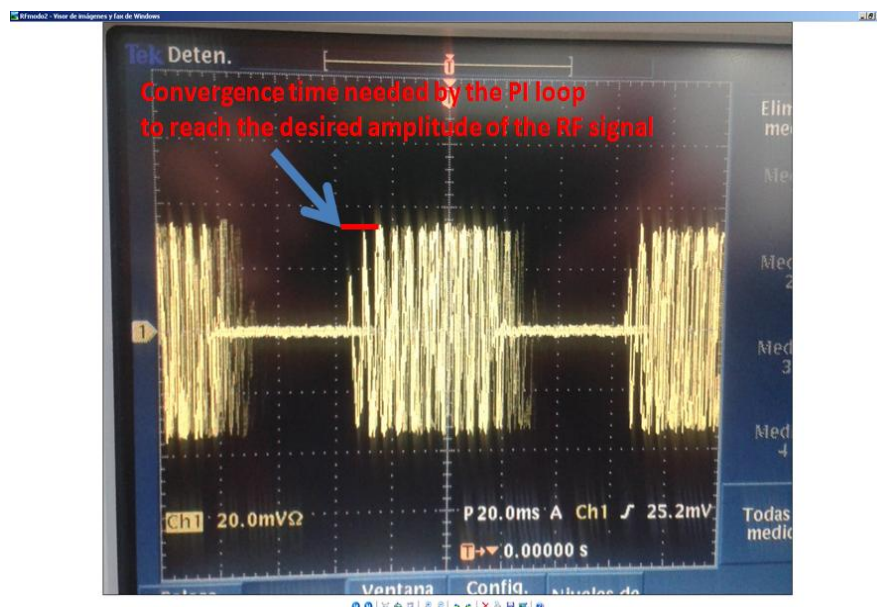


Figure 7.28: Image of RF signal generated in pulsed mode and closed loop. Pulse duration is 50 ms, which corresponds with the half of the period. PI loop convergence time can be observed

### 7.3 Tests on the RF Prototype Chain

The first RF platform chain manufactured, named as *RF Prototype Chain*, has been installed and extensively tested in order to show its full capabilities. These tests include the demonstration of the full power, linearity, emergency stop, amplitude and phase stability, as well as transient times. The purpose of this section is to show how some of these tests have been conducted satisfactorily and to present the role of the LLRF control system within the whole activity. LLRF system with the cPCI rack, the LOFE, the DIFE and the control system GUI, can be seen Fig. 7.29.

As explained in previous sections, LLRF system controls the amplitude and phase of 18 three-stage amplifier chains working at 175 MHz (8 chains, up to 200 kW, for the RFQ, 8 chains, up to 105 kW, for the SRF Linac and 2 chains more, up to 16 kW, for the MEBT). The prototype amplifier chain used in the following tests is able to reach a power of 220kW, that is enough to feed RF chains for RFQ and SRF Linac. RF chains for MEBT subsystem are based in solid state amplifiers [132] and it does not corresponds to the technology showed in the following sections but the control system operation, interface and behavior, is mostly the same.

For this thesis, the importance of the latter tests is not so much the numerical result or performance but once again, the role of the control system as the key to achieve any authentic operation in the system. The validity of the control system in real circumstances as the following, that will be equivalent to future situations of the whole accelerator operation, unequivocally certify the accurate development presented in this work.



Figure 7.29: RF Prototype Chain with LLRF system installed

RF prototype amplifier chain, see Fig. 7.30, contains the following devices:

- Two 19 inches standard racks with 46U, locating power supply units, LLRF system, solid state amplifiers, protection system, etc.
- Two TH561 tetrode based amplifiers
- Two TH781 tetrode based amplifiers
- Water and air cooling equipment
- Protection system equipment
- Circulator
- Load

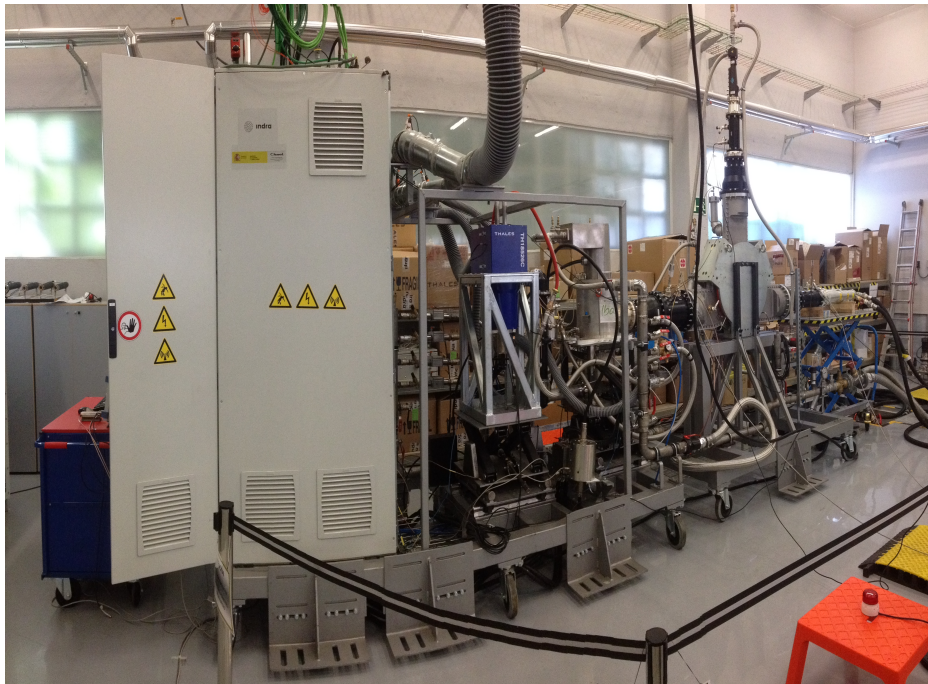


Figure 7.30: RF Prototype Chain side view

In order to enable maximum RF delivered power, the final amplifier has to be matched to the coaxial line impedance. Final amplifier is tested to deliver maximum RF output power loaded with  $50\Omega$  load.

Table 7.7 shows the tests and the target values that must be achieved to fulfill the acceptance conditions that ensure a proper operation of the system meeting the requirements of power and safety. In bold, the tests that have been chosen to be explained here, they are considered the most relevant for exhibiting the role of the control system within the entire prototype.

Table 7.7: Prototype RF chain acceptance conditions

Test	Target value
Operating frequency	175 MHz
Bandwidth	$\pm 250\text{kHz}@ - 1\text{dB}$
<b>Phase Stability</b>	(Closed Loop) $\pm 1\text{degree}$
<b>Amplitude Stability</b>	(Closed Loop) $\pm 1\%$ . 220KW
<b>Power Linearity</b>	(Closed Loop) 1%
<b>Maximum Output RF Power</b>	200kW CW
20kW CW Reflected Power	2 hours
<b>RF Power Emergency Stop</b>	$< 10\mu\text{s}$
200kW Reflected Power	$10\mu\text{s}$

### 7.3.1 Phase stability test

Defining a phase for a RF signal is one of the basic functions of the LLRF system. The stability of the phase RF signal is essential for the proper work of the system, in addition, phase signal is one of the parameters used to carry out the cavity tuning loop. The phase stability test is carried out for 15 minutes, and during this time, the rms (root mean square) jitter levels are measured each 1 minute. The phase stability for the RF chains must stand within a  $\pm 1$  degree interval. Previous tests and measurements have estimated that phase variations in 15 minutes are enough to conclude if the signal is stable or not.

To develop the test, first, LLRF interface must be configured in order to cut-off the signal at RF chain input if the forward or reverse powers in these points are higher than 5KW in Cavity Reverse, 5KW in Circulator Reverse and 5KW in Forward Load. Interface area where this parameters are configured is showed in Fig. 7.31.

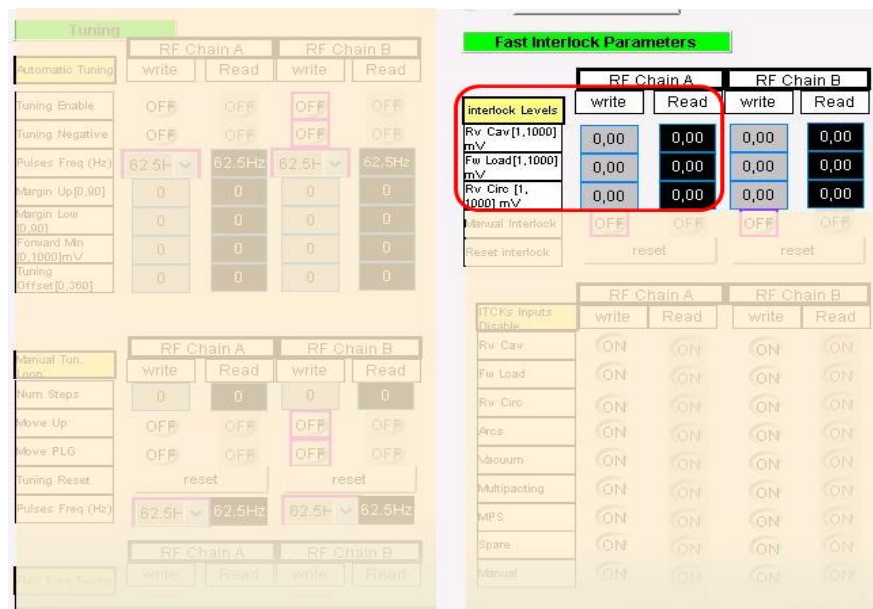


Figure 7.31: LLRF control system interface where interlocks thresholds are defined

System test set-up with an spectrum analyzer is shown in Fig. 7.32. The signal generator will be connected to the master oscillator input of the LLRF (MO IN). It must be configured in order to have a 175 MHz signal between -15 and 0 dBm at the LLRF MO input and the 10 MHz signal reference output (REF OUT) in the signal generator must be connected with the REF input in the LLRF.

Phase offset between two waves is the difference between their phases, defined as  $\phi = 2\pi\tau/T$ , which can be transformed into  $\phi = 2\pi f\tau$ . Jitter, measured in seconds, is the undesired deviation from true periodicity of an assumed periodic signal and corresponds to  $\tau$ , retardation respect to a nominal phase. The bigger the jitter, the more unstable the signal is. The worst jitter measured and displayed in Tab. 7.8 corresponds to 1.1421 ps. Then, phase offset  $\phi$  with worst jitter gives a result of 0.0015 radians (being  $f=175\text{MHz}$  and  $\tau=1.421\text{ps}$ ) which is equal to 0.0895 degrees, a tolerable phase offset value, within 1 degree interval.



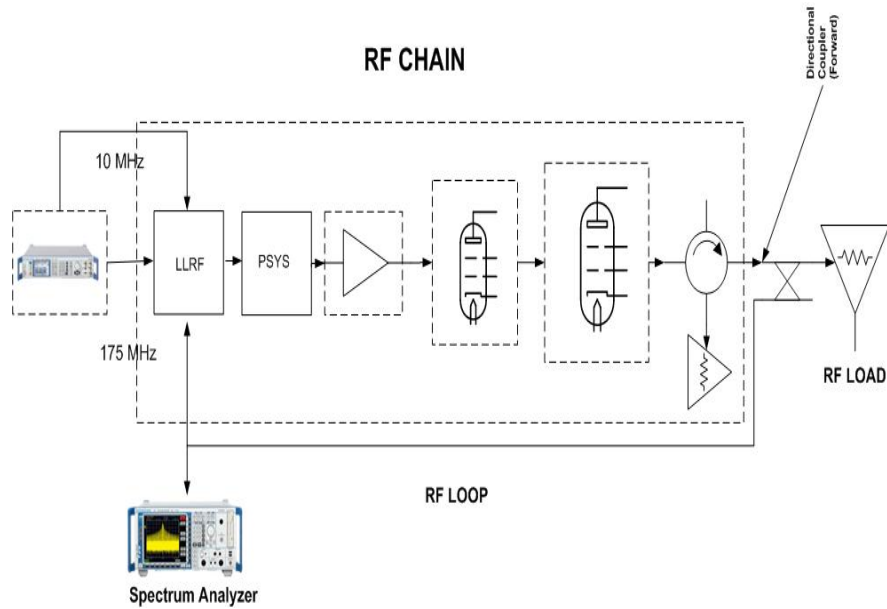


Figure 7.32: System configuration for the phase stability test

Table 7.8: Phase stability measurements in picoseconds

Time	rms Jitter (s)
T0	1.1255 ps
T0 + 1'	1.1283 ps
T0 + 2'	1.1156 ps
T0 + 3'	1.1128 ps
T0 + 4'	1.1151 ps
T0 + 5'	1.1121 ps
T0 + 6'	1.1234 ps
T0 + 7'	1.1271 ps
T0 + 8'	1.1275 ps
T0 + 9'	1.1231 ps
T0 + 10'	1.1421 ps
T0 + 11'	1.1207 ps
T0 + 12'	1.1371 ps
T0 + 13'	1.1411 ps
T0 + 14'	1.1271 ps
T0 + 15'	1.1383 ps

### 7.3.2 Amplitude stability test

The amplitude stability test consists in making the system work at full power for a certain amount (15 minutes) of time in order to see if variations in the stability of the maximum amplitude signal required are within the range of  $\pm 1\%$ . The stability of the amplitude RF signal is essential for the proper work of the system, in addition, amplitude is also one of the parameters used to carry out the cavity tuning loop.

To develop the test, the signal generator will be connected to the master oscillator input of the LLRF (MO IN). It is configured in order to have a 175 MHz signal between -15 and 0 dBm at the LLRF MO input. The 10 MHz signal reference output (REF OUT) in the signal generator must be connected with the REF input in the LLRF. Regarding to LLRF interface, it must be configured in the same way as before, in order to cut-off the signal at RF input if the forward or reverse powers are higher than the mentioned limits of 5KW. Main parameters must be modified in order to have 220 KW at the RF chain output with closed loop mode. During the test, it must be possible to see the positives and negatives variations, but only the maximum and minimum values are recorded. For that purpose, the power meter is configured with same probe in both of the measurements in order to see the positive and negative variations (around  $\pm 1\%$ ) at same time. In the *Meas Setup* menu, the maximum positive and negative variation are recorded. The limits must be written between 100% and 101% and between 99% and 100%

The system scheme with the power meter ready for the test can be seen in Fig. 7.33.

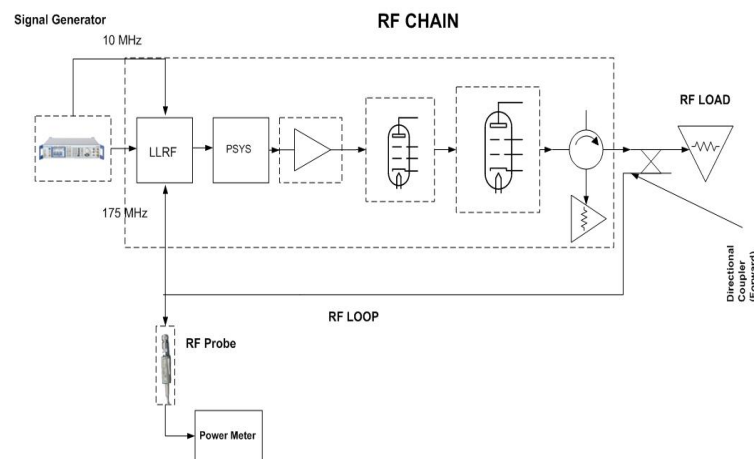


Figure 7.33: System scheme used both in the amplitude stability test and in the power linearity test

Running the test for 15 minutes at 220kW yields a result between the desired  $\pm 1\%$  interval. Only the worst values are recorded and taken into account:

- Worst case for negative variation = 0.2%, 219.54 KW measured.
- Worst case for positive variation = 0.4%, 220.88 KW measured.

### 7.3.3 Power linearity test

As a general definition, a system can be considered linear if the relationship between the input and the output of the system is a linear map: If input  $x_1(t)$ , produces response  $y_1(t)$ , and input  $x_2(t)$ , produces response  $y_2(t)$ , then the scaled and summed input  $a_1x_1(t) + a_2x_2(t)$ , produces the scaled and summed response  $a_1y_1(t) + a_2y_2(t)$ , where  $a_1$  and  $a_2$  are real scalars. In the linearity test exposed in this section, relationship between input ideal power ( $P_{configured}$ ) and output real power ( $P_{measured}$ ) must be linear between  $\pm 1\%$ .

To develop the linearity test, LLRF system must be configured again in closed loop mode. After that, different power values at RF chain output must be programmed in the LLRF interface. For each programmed level the real value at output must be measured using the power meter. This system test set-up corresponds with the scheme showed in Fig. 7.33.

First, systematic error is calculated. Sources of systematic error may be imperfect calibration of measurement instruments or imperfect methods of observation, systematic error is common to all measurements. The *relative error* to each measurement is calculated, see Tab. 7.9 for relative error measurements, with:

$$RelativeError = ([P_{configured} - P_{measured}] / P_{configured}).$$

Table 7.9: Relative error measurements

Power configured	Power measured	Error(relative)
20 kW	19.75 kW	0.0125
40 kW	39.57 kW	0.0107
60 kW	59.30 kW	0.0116
80 kW	79.13 kW	0.0108
100 kW	98.87 kW	0.0113
120 kW	119.3 kW	0.00583
140 kW	138.1 kW	0.0135
160 kW	158.1 kW	0.0118
180 kW	177.8 kW	0.0122
200 kW	197.8 kW	0.011
220 kW	217.5 kW	0.0113

Then, the *average error* is obtained with:

$$AverageError = \Sigma RelativeError / 11 = 0.0103.$$

Normalized measurements are listed in Tab. 7.10. Values indicated as  $P_{normalized}$ ,  $P_{measured} / P_{configured}$ , are compared with the *Bottom limit*,  $([1 - AverageError] * 0.99)$ , and *Top limit*,  $([1 + AverageError] * 1.01)$ , which are the normalized bounds taking into account the average error. Finally, A linear fit of the normalized measurements can be seen in Fig. 7.34.



Table 7.10: Linearity measurements

Power configured	Power normalized	Bottom limit	Top limit
20 kW	0.987 kW	0.979	0.999
40 kW	0.989 kW	0.979	0.999
60 kW	0.988 kW	0.979	0.999
80 kW	0.989 kW	0.979	0.999
100 kW	0.988 kW	0.979	0.999
120 kW	0.994 kW	0.979	0.999
140 kW	0.986 kW	0.979	0.999
160 kW	0.988 kW	0.979	0.999
180 kW	0.987 kW	0.979	0.999
200 kW	0.989 kW	0.979	0.999
220 kW	0.989 kW	0.979	0.999

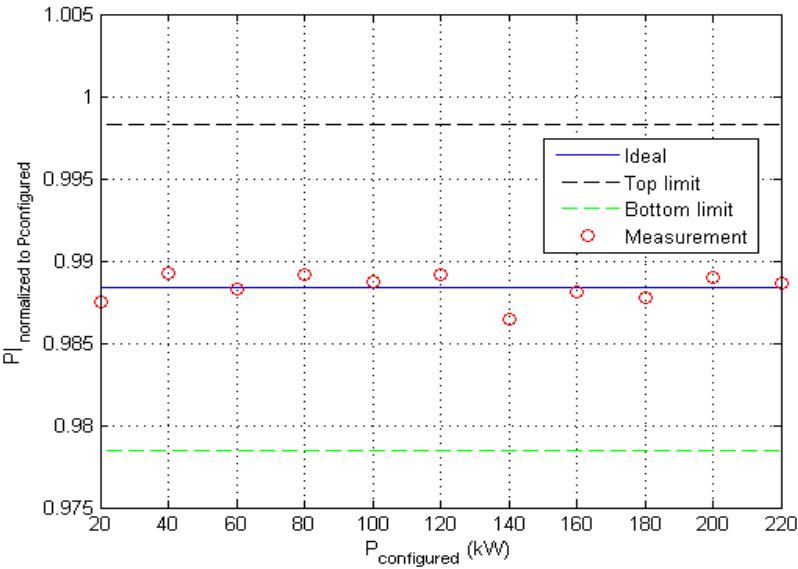


Figure 7.34: Image showing top limit and bottom limit in comparison with the fitted normalized measurements

### 7.3.4 Maximum output RF power test

The RF chain must properly work at maximum power for a minimum of 2 hours. The output level must stand within  $\pm 1\%$  after 2 hours and it must work without alarms or malfunctions. Previous tests and measurements have estimated that maximum power deviations in 2 hours can be enough to conclude whether the system can work at maximum power for longer periods.

To carry out this test, a 220KW signal is defined through the LLRF control system interface. Each 15 minutes the output power is recorded, this is another way of measuring the amplitude stability in the RF chain at maximum power. Measurements obtained are detailed in Tab. 7.11. As it can be observed they are oscillating inside the  $\pm 1\%$  margin. It can be concluded that the entire system works at maximum power and for a long period within the range required.

Table 7.11: RF maximum power measurements

Time	Min. Deviation from nominal output (%)	Max. Deviation from nominal output (%)
T0	100.0	100.0
T0 + 15'	99.96	100.4
T0 + 30'	99.93	100.4
T0 + 45'	99.84	100.4
T0 + 1h	99.80	100.4
T0 + 1h 15'	99.80	100.4
T0 + 1h 30'	99.80	100.4
T0 + 1h 45'	99.80	100.4
T0 + 2h	99.80	100.4

### 7.3.5 RF emergency stop test

As explained before, a fast interlock system is integrated in the LLRF. This safety system will prevent the RF chains sending power to the accelerator cavities in case there is an interlock alarm, by means of cutting off the RF signal generated. General purpose input/output (GPIO) connectors are connected to pull up resistors. This implies that when a pin is configured as an input and no cable is connected, FPGA boards read a logic 1, for safety issues, that state is considered an interlock. When there is no interlock, the device connected to the GPIO should force this signal to be 0.

In order to secure the system, RF power must be switched off in less than  $< 10\mu s$ . This emergency stop system do not have software processing but hardware direct links and a pin switch. LLRF control system role in an emergency stop is to inform the operator about the interlocks status, i.e., kind of interlock/s detected and to show the list of actions carried out to secure the system. In addition, the LLRF interface is configured in order to cut-off the signal if the forward or reverse power in these points are higher than certain values, thus, it is also a good way to try if the thresholds entered through the interface are properly acquired and if the diagnostics are correctly shown after the emergency stop.

To carry out this test, the power at RF chain output is configured at 220 KW (closed loop mode), a test option in the arc detector system is then forced using its interface, simulating an interlock signal. The system scheme is showed in Fig. 7.35.

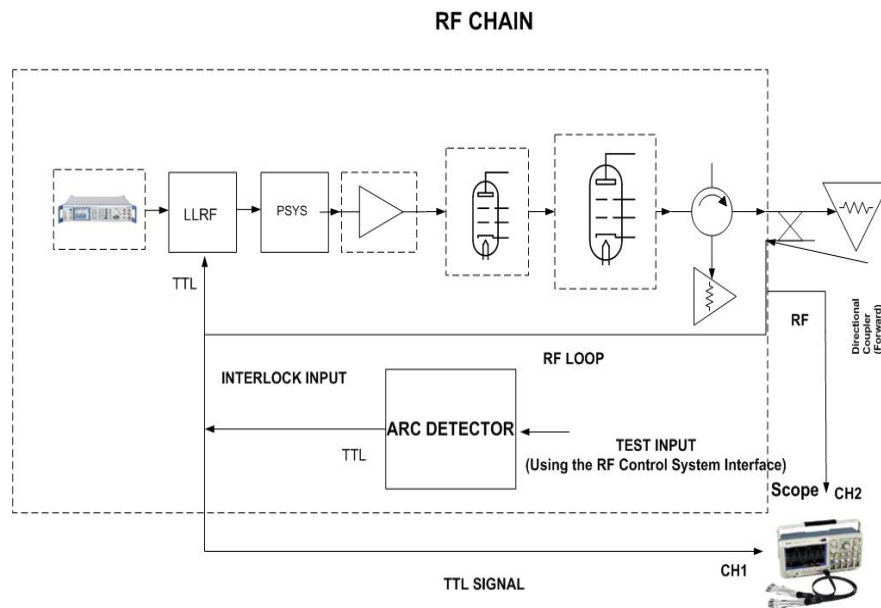


Figure 7.35: System scheme for the emergency stop test

In Fig. 7.36,  $t_1$  corresponds to 0s, the interlock signal is detected;  $t_2$  is  $7.64\mu s$ , it corresponds to the moment when the power is 0, the system is then secured in less than  $< 10\mu s$ .

The actions performed by the LLRF system after the arc interlock alarm detected for this test, are displayed in Fig. 7.37. If all interlock leds switch to red, ON, it means that

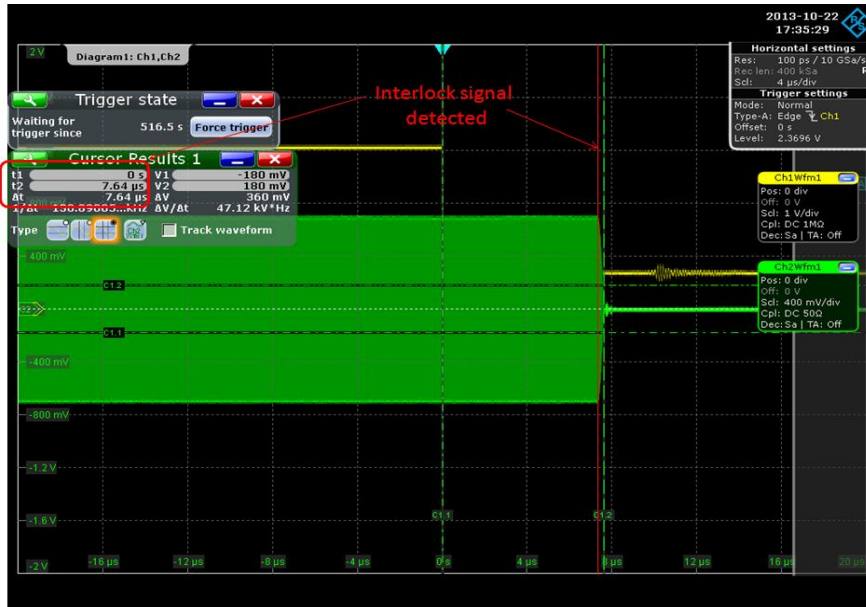


Figure 7.36: RF emergency stop at 220 kW, time consumed  $7.64\mu\text{s}$

all possible actions have been automatically achieved by the LLRF system after the interlock alarm, DACs OFF, pin switch, trigger to FDL and interlock alarm sent to RF PLC and MPS. As explained in previous sections, the list of actions carried out by the LLRF system is configurable by the operator through the LLRF GUI, see sections 6.4.4.9 and 7.2.1.2 for more details.

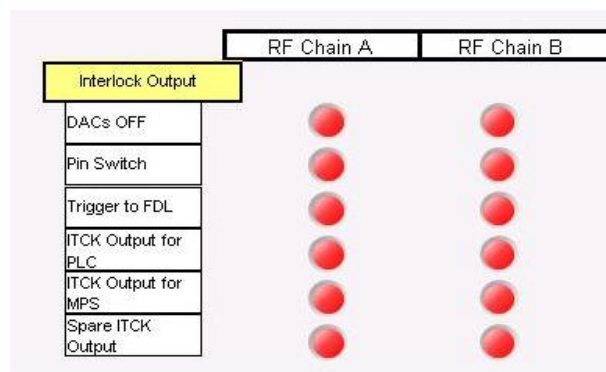


Figure 7.37: List of actions showed in the GUI and performed by the LLRF when an interlock is detected. When the led is red means the action has been executed

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# 8

## Conclusions

*No se observe demasiado. No extraiga conclusiones precipitadas de lo que ocurre; deje que simplemente suceda*

*Cartas a un Joven Poeta*, Rainer María Rilke.

### 8.1 Introduction

Modern control systems have become essential tools for the operation of large facilities, especially of particle accelerators in any of its possible uses. Among all possible control architectures, the distributed option provides a capacity of more efficient operation, however, its design and implementation are more complex.

The large control systems are divided into subsystems, which are divided, in turn, on devices. Each device responds to different needs that are established by a number of requirements that are derived from the fundamental objectives of the facility itself. The objectives and requirements of LIPAc have been explained and cited throughout the document and they are the rationale for each of the architectures of each of the local control systems. Full integration and understanding of all these parts is always achieved at the level of the control system. To this end the aid of a distributed control tool becomes fundamental.

In this thesis, to provide better accelerator operation, all architectures and designs submitted should follow a distributed structure and must speak the same language, that is, to share the same software. For this, the main instrument used in the control system development is EPICS, an independent software toolkit, extremely adaptable and expandable.

The ability to make EPICS run in each of the devices and subsystems presented is not trivial, but the benefits provided against other centralized solutions are absolutely overwhelming. A large facility like LIPAc, whose operation opens unstudied ways, cannot be conceived with independent subsystems, centralized at a single point or unable to understand each other.

The operation of a particle accelerator as LIPAc is only possible with a control system that manages the flow of the control parameters within milliseconds. Both the machine itself and the operators should be aware of what is happening in each of the parts of the accelerator, in order to execute the most optimal performance for each case, avoiding both personal and economic damage, and achieving a more efficient and durable operation.

The control architecture proposed in this work provides the following advantages:

- Easily scalable, open architecture. It is easy to implement and expand the system changes.
- It is a standards-based architecture for all subsystems. In this way it is possible for all devices to communicate with each other as long as they have one certain characteristics.
- The control process of the subsystems can be accomplished from a central location or, with the appropriate information, from different points distributed in each local control system. This improves overall system performance and the ability to intervene in case of stop.
- Each of the parameters that are used to operate the accelerator and each of the signals necessary to know their status, have a unique name that makes possible to understand what is going on at all times and where is going.

The LIPAc distributed control system has its own characteristics that make it different to any other system. LIPAc inherent characteristics require a large amount of data to be processed in the control system at every moment. Therefore, communication between the different layers of each control subsystem, from interface layer to instrumentation one, has to be prompt and appropriate to avoid inconsistencies or delays in the readings/writings signals.

The signals have to travel from the outer layer of the subsystem to the innermost layer, and they have to do that in the fastest way possible. To carry out these functions is necessary to consider a hardware architecture that uses fast and stable IOCs, enabling the system to to survive any failure of a given controller.

## 8.2 Contributions made

As exposed in the introduction section, several objectives which represent a number of questions related with the design and implementation of a control system for a particle accelerator with a single general attributes have been established. The work presented meets these objectives in the following way:

A general description of LIPAc is displayed, both from the point of view of installation and the accelerator system, describing each of the subsystems that comprise it, LIPAc beam power provides unique characteristics that make the control system an unique and heterogeneous elaboration. For each of the subsystems exposed, its local control system design has been revealed, explaining the main features and showing their architecture. Local control systems follow a ratified distributed architecture and properly respond to the specific function for which they are designed, however, they are not isolated entities, they communicate with each other and follow the same multilayer structure. Local control systems for MEBT, HEBT and BD, SRF Linac, RF and BI have been mostly designed in the framework of this thesis. They are composed of different devices but capable of being operated from anywhere in the accelerator and in a standard manner. Since there is no previous experience in operating a machine like

LIPAc, all EPICS PVs must be available for the central control system, which is the one and only that can manage the whole accelerator and can take decisions based on the information given from every subsystem. Making all the PVs visible for the central control system means to develop an EPICS based control system for each device, that is, different solutions for a global understanding.

The development of the LLRF EPICS based control system is also elucidated. This is one of the most delicate parts of the accelerator which has several interfaces with critical subsystems. The solution described in this thesis proposes an unprecedented architecture and compared to other similar developments, it provides more functionalities.

A fast and accurate communication between FPGA and EPICS is showed in the PVs tests and in the simulated operation situations. LLRF system test bench working on different modes of operation demonstrates the flexibility and the efficiency of the LLRF control system in order to produce RF signals with real-time adjustable parameters.

The successful testing of phase and amplitude stability, linearity, full output RF power and emergency stop on the RF Prototype Amplifier Chain, shows that the LLRF control system fulfills its function, being able to operate the system through in real situations with full solvency and safety.

### 8.3 Publications of the author related with this work

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